Design and Simulation of a Low-Power Two-Stage Operational Transconductance Amplifier

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Abstract – This paper describes the design and simulation of a low-power two-stage operational transconductance amplifier (OTA) using a 0.18µm CMOS technology and a 1.8V power supply. It is shown that with careful design, a low-frequency gain greater than 70dB can be achieved together with high phase margin (greater than 45°), fast settling time (less than 40 ns), and low power consumption (0.467 mW).

I. Introduction

A systematic procedure for the design of a two-stage amplifier is presented in this report that describes how the values of the various circuit components can be derived from the provided specifications. Table I is a summary of the various OTA specifications that have to be met. Results obtained from simulations of the final design are also shown for comparison.

Fig. 1 shows the schematic of the OTA circuit used in this design. To achieve the high gain required a two-stage design is used. An NMOS input differential amplifier is followed by a PMOS common source amplifier. Miller compensation with nulling resistor is used to obtain the required phase margin. Other architectures such as cascoded and telescopic differential stages were considered for this design but were not selected since their advantages would be compromised by factors such as loss of swing headroom for a 1.8V design and increase in power consumption.

The design approach used in this project is based on the g_m/I_d technique. Additionally, instead of relying on textbook formulas for various quantities, pre-simulated technology characterization charts were used for better accuracy.

Table I. Summary of design specifications.

		Specification	This Design
DC small-signal gain		> 70 dB	74.25 dB
Input-referred offset		< 10 µV	-1.6 µV
Input V_{cm} range		[0.75, 1.05]	[0.75, 1.05]
Output swing		[0.3, 1.5]	[0.275, 1.56]
Unity gain frequency		> 100 MHz	101 MHz
Phase margin		> 45°	55°
Power Consumption		< 1 mW	0.467 mW
Settling time	Up	< 40 ns	21.4 ns
	Down	< 40 ns	32.4 ns
CMRR at DC		> 70 dB	70.35 dB
PSRR at DC		> 70 dB	76.8 dB

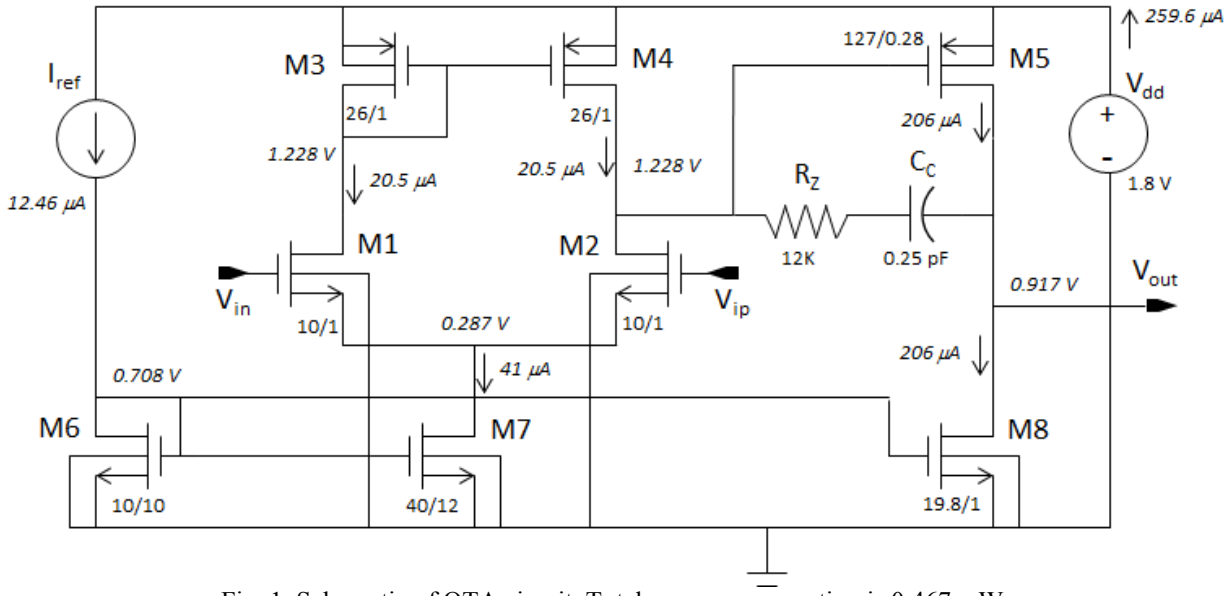


Fig. 1. Schematic of OTA circuit. Total power consumption is 0.467 mW.

II. THEORY BASED DESIGN

In this section the sizing and values of various components used in the OTA design are derived from theoretical analysis. These serve as the starting point of Spice simulations.

The two-stage OTA of Fig. 1 is a system consisting of a single zero and three poles. Its transfer function can be written as [1]:

$$A(s) = A_{v0}\frac{\left(1-\frac{s}{z_1}\right)}{\left(1-\frac{s}{p_1}\right)\left(1-\frac{s}{p_2}\right)\left(1-\frac{s}{p_3}\right)}, \quad (1)$$

where A_{v0} is the dc gain given by

$$A_{v0} = \frac{g_{m2}g_{m5}}{(g_{ds2}+g_{ds4})(g_{ds5}+g_{ds8})}, \quad (2)$$

z_1 is a zero given by

$$z_1 = \frac{1}{C_c\left(\frac{1}{g_{m5}}-R_z\right)}, \quad (3)$$

and p_1, p_2, and p_3 are the three poles of the system given, respectively, by

$$p_1 = -\frac{1}{\frac{C_1+C_c}{g_{ds24}}+\frac{C_2+C_c}{g_{ds58}}+\frac{g_{m5}C_c}{g_{ds24}g_{ds58}}} \quad (4)$$

where $g_{ds24} = (g_{ds2} + g_{ds4})$ and $g_{ds58} = (g_{ds5} + g_{ds8})$,

$$p_2 = -\frac{g_{m5}}{C_1+\left(\frac{C_1}{C_c}+1\right)C_2}, \quad (5)$$

and

$$p_3 = -\frac{1}{R_zC_1}. \quad (6)$$

In equations (4), (5), and (6) C_1 and C_2 represent, respectively the input capacitance of the second common source stage, and the total load capacitance. It can be assumed that C_1 is equal to C_{gs5} and C_2 is equal to the load capacitance C_L plus ($C_{db5} + C_{db8}$).

The design strategy used in this work is to choose C_c and R_z such as to cancel the non-dominant pole at p_3 with the zero, resulting in a second order (two pole) transfer function. Secondly, if these can be chosen such that the remaining non-dominant pole p_2 is placed at or near the desired unity gain frequency then it can be expected that sufficient phase margin will remain. As a result of this strategy the OTA transfer function effectively becomes equal to

$$A(s) = \frac{A_{v0}}{\left(1-\frac{s}{p_1}\right)\left(1-\frac{s}{p_2}\right)}. \quad (7)$$

The loop gain expression then is

$$T(s) = \frac{\beta A_{v0}}{\left(1-\frac{s}{p_1}\right)\left(1-\frac{s}{p_2}\right)}, \quad (8)$$

where β is the "return factor". For this project β is 0.5, assuming the OTA's input capacitance is negligible compared to feedback (C_f) and sampling capacitance (C_s).

At the unity gain frequency ω_u, $|T(s)| = 1$. From (8) it can be shown that

$$A_{v0}^2\beta^2\omega_{p1}^2 = \omega_u^2\left(1+\frac{\omega_u^2}{\omega_{p2}^2}\right). \quad (9)$$

Equation (9) provides a relation between the two poles of the system and the desired gain and unity gain frequency.

The phase margin (PM) is the additional phase required to bring the phase of $T(s)$ to 180. It is given as

$$PM = 90° - \tan^{-1}\left(\frac{\omega_u}{\omega_{p2}}\right). \quad (10)$$

The closed loop transfer function of this two-pole system is given by

$$H(s) = \frac{A_{v0}p_1p_2}{s^2+s(p_1+p_2)+p_1p_2(1+\beta A_{v0})} \quad (11)$$

from which the unit step response, assuming a linear system, is obtained as

$$S(t) = \left(\frac{A_{v0}}{1+\beta A_{v0}}\right)\left(1-e^{-\rho t}\frac{\sin(\mu t+\phi)}{\sin(\phi)}\right), \quad (12)$$

where

$$\rho = \frac{1}{2}\left(\omega_{p1}+\omega_{p2}\right), \quad (13)$$

$$\mu = \frac{1}{2}\sqrt{4\beta A_{v0}\omega_{p1}\omega_{p2}-\left(\omega_{p1}-\omega_{p2}\right)^2}, \quad (14)$$

and

$$\sin(\phi) = \frac{\mu}{\sqrt{\mu^2+\rho^2}}. \quad (15)$$

Using the decay envelop function of (12), i.e. ignoring the sinusoidal oscillation term, gives the settling time t_s as

$$t_s = t_{slew} - \frac{1}{\rho}\ln(\varepsilon_{d,tol}), \qquad (16)$$

where the dynamic error tolerance $\varepsilon_{d,tol}$ is 0.1% and

$$t_{slew} = \frac{|V_{xstep}| - 2.8/(g_{m2}/I_{d2})}{\beta \times SR}. \qquad (17)$$

The terms V_{xstep} and slew rate SR in (17) are given as follows:

$$V_{xstep} = V_{idstep}\frac{C_s}{C_s + C_f}, \qquad (18)$$

and

$$SR = \frac{I_{d7}/2}{C_c}. \qquad (19)$$

The theoretical design of the two-stage OTA is completed using the expressions given above for the various characteristics. The manner in which this is done is described next.

First, it is noted that for a maximum power dissipation of 1 mW with a 1.8V supply voltage, the total current budget has to be limited to 555 μA. Next, since a DC small signal gain of about 3162 (70 db) is desired, it is meaningful to aim for gain of √3162 = 56 in each of the two stages. For the architectures used in the two stages, this implies an intrinsic gain (g_m/g_{ds}) of about 112 for each stage. The logic behind this is as follows. Referring to Fig. 1, the gain of the differential stage is given as $g_{m2}/(g_{ds2} + g_{ds4})$. Assuming roughly equal g_{ds} in M2 and M4, the low frequency gain of the differential amplifier can be approximated as one-half of its intrinsic gain. Therefore, to get a gain of 56, an intrinsic gain of 112 is desired. The same reasoning is applicable to the common-source stage. To achieve this level of intrinsic gain in the NMOS input differential stage, it is decided to use L = 1 μm for M1 and M2. The same L is used for the PMOS load transistors M3 and M4 in order to keep their output conductance low. From technology charts generated for L = 1 μm, it is found that an intrinsic gain of about 112 occurs at g_m/I_d of about 6. In order to keep some margin it is decided to use a g_m/I_d of 13 which corresponds to an intrinsic gain of 126. Furthermore, in order to conserve power, it is decided to use a tail current of roughly one-tenth of the total current budget, i.e. I_{tail} = 50 μA. Since the I_d/W from technology charts at g_m/I_d of 13 is 2.4 μA/μm for L = 1 μm, the necessary width for M1 and M2 works out to 10.4 μm. The widths of the PMOS transistors M3 and M4 are estimated in a similar manner assuming they operate at the same g_m/I_d of 13. The corresponding I_d/W from PMOS technology charts is 0.675 μA/μm, which implies the width needed for M3 and M4 is 37 μm. Since I_d, g_m/I_d, and g_m/g_{ds} are known for these transistors, it is possible to estimate g_m and g_{ds} of M1 - M4. This gives $g_{m1} = g_{m2} = g_{m3} = g_{m4}$ = 0.325 mS, $g_{ds1} = g_{ds2}$ = 2.58 μS, and $g_{ds3} = g_{ds4}$ = 2.32 μS. From this information the low frequency gain of the differential stage is estimated to be 66, i.e. 36.4 dB.

For the common-source stage it is recognized that in addition to providing the remaining DC gain, M5 will influence the location of pole p_2. From (5) it is noted that the location of p_2 can be increased by increasing g_{m5} and keeping C_{gs5} low. Increasing the width of M5 helps increase its g_m but also increases its C_{gs} and its bias current. Thus, it is better to reduce the length of M5. However, it should be kept in mind that lowering L results in a loss of intrinsic gain g_m/g_{ds}. It was decided to back off from the minimum channel length and as a compromise L = 0.28 μm was chosen for M5. Using similar reasoning as for the differential stage, a g_m/I_d of 16 was selected to give an intrinsic gain g_{m5}/g_{ds5} of about 100 and a I_d/W of 1.6 μA/μm.

Next, an approximate value of g_{m5} can be estimated from (5) assuming $C_2 = C_L$, ignoring the effect of C_1, and taking p_2 to be located at 4x the desired unity gain frequency of 100 MHz. Since C_L = 1 pF, the resulting value of g_{m5} is 2.5 mS. To provide some additional design margin g_{m5} = 3 mS is used. This results in a I_d of 187 μA which is rounded up to 200 μA and g_{ds5} of 25 μS. The required width of M5 then is 125 μm.

The sizes of the remaining transistors, M6 - M8, and the reference current are fixed next. I_{ref} is chosen to be 50 mA, equal to the tail current of the differential stage. M6 and M7 are sized as 40/10. The long channel length allows the tail

resistance to be kept at a high value which helps CMRR. Since M8 needs to carry 4x the reference current it needs a 4x larger W/L ratio. Increasing its W to 160 would result in a large C_{db8} which would add to the load on the OTA. Instead, a 16/1 size is chosen for M8. Since M8 carries 200 μA, its I_d/W is 12.5 μA/μm which implies a g_m/I_d of 5.8 V^{-1} and g_m/g_{ds} of 111 from the technology charts. From this g_{ds8} = 10.5 μS. The low frequency gain of the common source stage is given by g_{m5} /(g_{ds5} + g_{ds8}) and equals 84.5 (i.e. 38.5 dB). The total OTA low frequency gain then works out to 74.9 dB which exceeds the 70 dB specification.

The last remaining part of the design is to estimate values for the compensation capacitor C_c and the nulling resistor R_z. To estimate a value for C_c the location of the pole p_1 is first estimated as $\omega_u/(\beta A_{v0})$ = 35.7 kHz. Then from (4) C_c is approximated as:

$$C_c \approx \frac{1}{2\pi}\frac{(g_{ds2}+g_{ds4})(g_{ds5}+g_{ds8})}{p_1 g_{m5}}. \quad (20)$$

Inserting the previously obtained values for the various quantities on the right hand side of (20) gives C_c of 259 fF. Since the strategy used in this design is to attempt to cancel the p_3 pole with the zero, the required value of R_z can be estimated by equating (3) and (6). The result is:

$$R_z = \frac{C_c}{g_{m5}(C_c - C_1)}. \quad (21)$$

C_1 can be approximated as C_{gs5}, which in turn can be found from the transit frequency (f_T) plots on the technology charts. Since g_m/I_d of M5 was previously estimated as 16, the corresponding f_T value for L = 0.28 μm is 3.5 GHz. C_{gs5} is then obtained as $g_m/(2\pi \text{ x } f_T)(\ C_{gs5}/\ C_{gg5})$ = 250 fF. Using this value in (21) gives R_z = 9.7K.

Since the values of all elements of the design are now available, it is useful to compute the locations of the various poles and zeroes to ensure that the assumptions made during the design procedure are satisfied. Using equations (3) - (6) the calculated pole and zero values are as follows:

f_{p1} = -34.6 kHz
f_{p2} = -215.5 MHz
f_{p3} = -65.37 MHz
f_{z1} = -65.37 MHz

Regarding CMRR, which is the ratio of the differential mode gain to the common mode gain (A_{cm}), it is sufficient to compute this ratio for the differential stage only. The differential mode gain of this stage is already shown to be 36.4 dB. The common mode gain is given by $g_{ds7}/(2g_{m3})$. g_{ds7} is estimated in the following manner. M7 is designed to carry 50 μA and has a width of 40 μm, implying a current per width of 1.25 μA/μm. From the technology charts the value of lambda at this I_d/W is 0.13 V^{-1} for an NMOS transistor with L = 1. Since M7 has L = 10, its lambda in reality will be lower than this value. Therefore, g_{ds7} will be no higher than 0.13 times I_{d7}, i.e. 6.5 μS. This implies A_{cm} will be at most -40 dB since g_{m3} is known to be 0.325 mS and the CMRR will be greater than 76.4 dB.

Values of various additional circuit specifications can now be calculated using the expressions given earlier in this section. These hand-calculated values are summarized in the Table II. It is noted that the unity gain frequency is slightly lower than than desired. At this stage it is considered close enough. During the final tuning of the design using Spice the unity gain frequency will be increased to meet or exceed the specification value (e.g. by increasing g_{m5}).

Table II. Summary of hand calculated values of various design specifications.

		Specification	Hand calculation
DC small-signal gain		> 70 dB	74.9 dB
Unity gain frequency		> 100 MHz	90 MHz
Phase margin		> 45°	67.4°
Power Consumption		< 1 mW	0.54 mW
Settling time	Up	< 40 ns	22 ns
	Down	< 40 ns	22 ns
CMRR at DC		> 70 dB	76.4 dB

III. Simulation Results

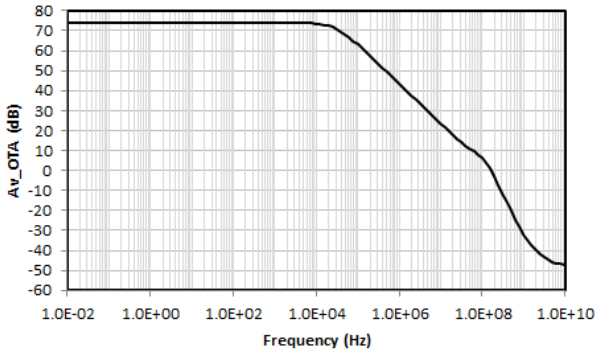
Upon completion of the initial design, the schematic of the OTA is input into Cadence and simulated. Some minor adjustments are made to bring the various specifications within their acceptable values / ranges. The main adjustments needed were in the sizing of M3 and M4 as well as M8 in order to reduce the input referred offset voltage to under the specified 10 μV limit and to increase g_{m5} so as to able to meet the minimum

unity gain frequency requirement. R_z also had to be adjusted to meet the settling time requirement. Table III lists the initial and final sizes of the various transistors.

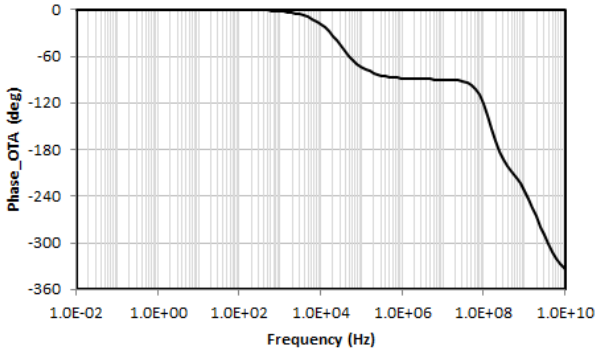
Table III. Comparison of the initial and final sizes and component values.

Component	Initial Value	Final Value
M1	10.4/1	10/1
M2	10.4/1	10/1
M3	37/1	26/1
M4	37/1	26/1
M5	125/0.28	127/0.28
M6	40/10	10/10
M7	40/10	40/12
M8	16/1	19.8/1
Rz	9.7K	12K
Cc	259 fF	250 fF
Iref	50 µA	12.46 µA

Fig. 2 shows the open-loop frequency response of the OTA. The open-loop gain of the OTA is 74.25 dB. The unity gain frequency is 169 MHz and the phase at this frequency is -157 degrees.



(a)



(b)

Fig. 2. Frequency response of OTA: (a) magnitude, (b) phase.

Fig. 3 shows the setup used to obtain the loop gain frequency response. An "iprobe" element (not shown in Fig. 3) is inserted in series with the feedback capacitor in order to run a stability analysis.

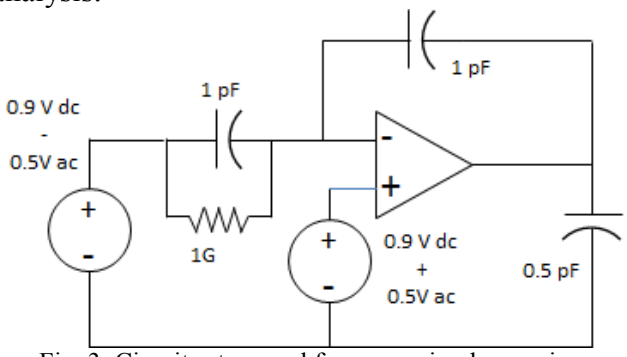
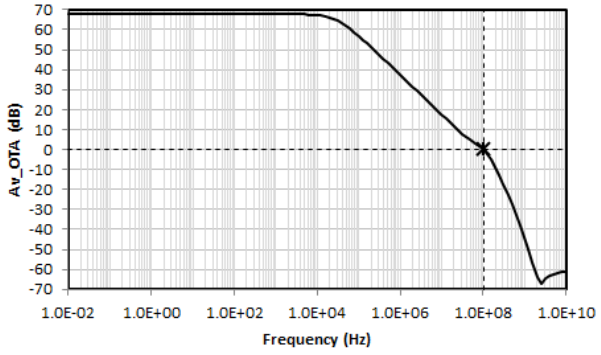
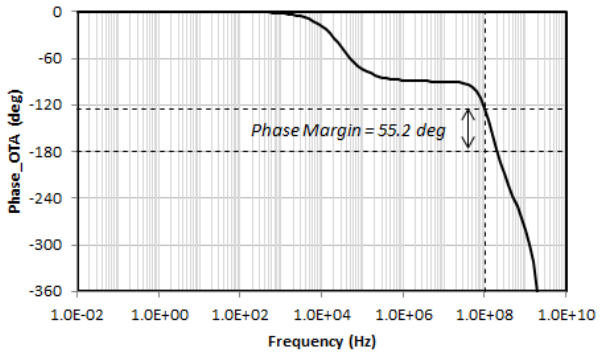


Fig. 3. Circuit setup used for measuring loop gain.

Fig. 4. shows the corresponding results obtained from a stability analysis. The unity gain frequency is 101 MHz and the phase at this frequency is -124.8 degrees, implying a phase margin of 55.2 degrees.



(a)



(b)

Fig. 4. Loop gain frequency response: (a) magnitude, (b) phase.

Fig. 5 shows the setup used to measure settling times from the output voltage transient. Settling times are measured for both an upward going step input (0.9V to 1.5V in 10 ps risetime) as

well as a downward going step input (0.9V to 0.3V in 10 ps risetime).

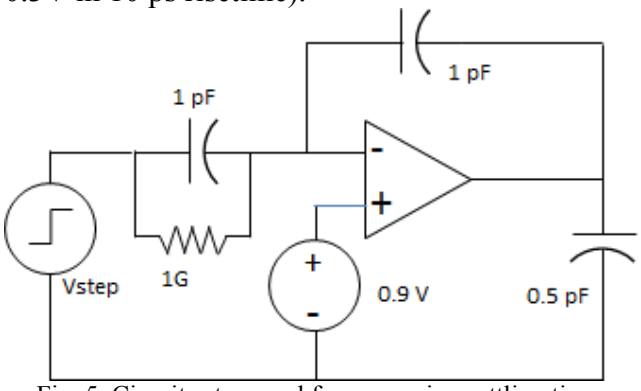
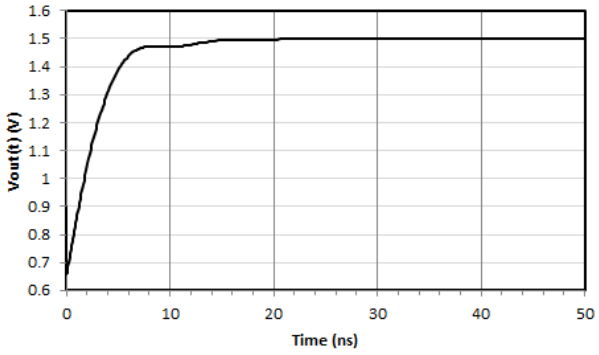
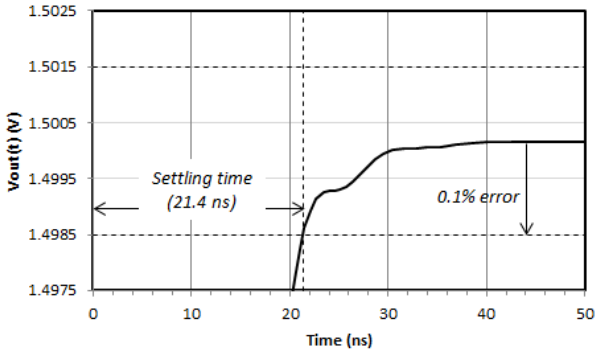


Fig. 5. Circuit setup used for measuring settling time.

Fig. 6. shows the output voltage settling time obtained from a transient analysis for a downward going input step. The settling time for this case is found to be about 21.4 nanoseconds.



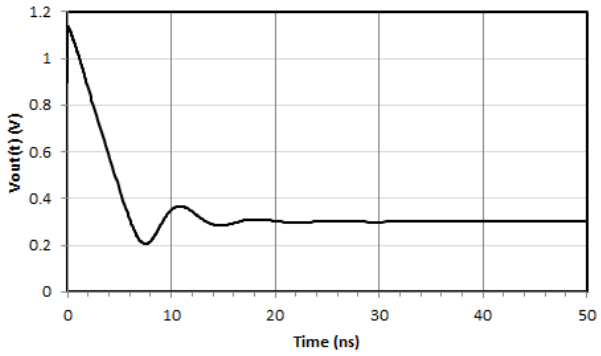
(a)



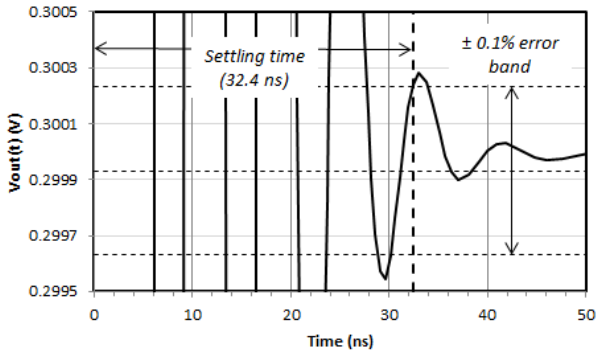
(b)

Fig. 6. Output voltage transient for a downward going input step function. (a) is expanded view and (b) is a zoomed in view.

Fig. 7 shows the output voltage settling time obtained from a transient analysis for an upward going input step. The settling time for this case is found to be about 32.4 nanoseconds. As expected from theory the settling transients show some oscillations. These oscillations are clearer in Fig. 7. The period of the oscillation obtained from simulations is about 140 MHz. In comparison, the theoretically expected frequency from (14) is about 100 MHz.



(a)



(b)

Fig. 7. Output voltage transient for a upward going input step function. (a) expanded view and (b) zoomed in view.

Fig. 8 shows the OTA DC gain as a function of output voltage. The values of the output voltage at which the gain drops to 67 dB are taken as the limits of the output swing. From the simulated results it is seen that the output swing is [0.275, 1.56].

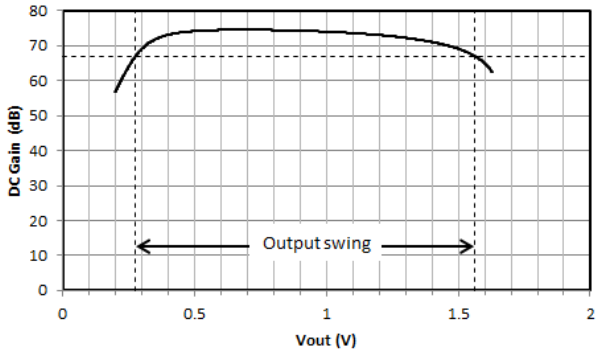


Fig. 8. OTA gain as a function of output voltage.

Fig. 9 shows the gain of the OTA as a function of the input common mode voltage. It is seen that over the range of the desired input common mode range the gain does not change appreciably.

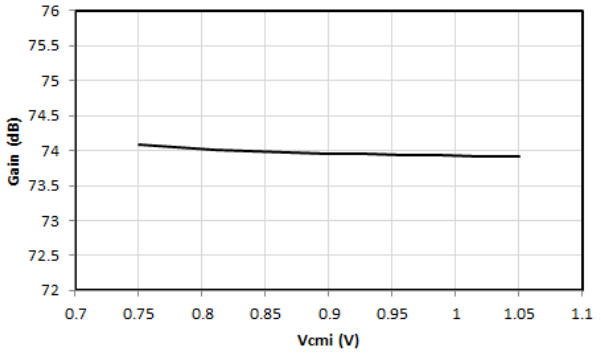


Fig. 9. OTA gain as a function of input common mode voltage.

Fig. 10 shows the CMRR behavior of the OTA. It is seen that at low frequencies the CMRR is 70.35 dB.

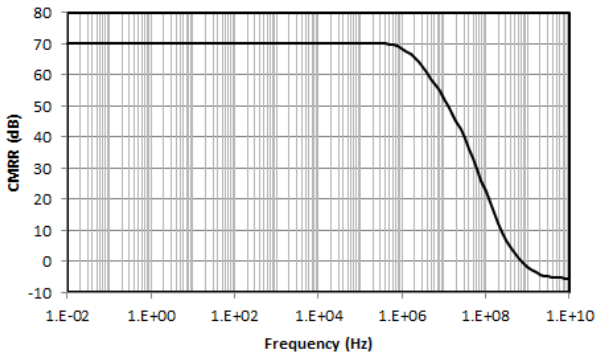


Fig. 10. OTA CMRR as a function of frequency.

Fig. 11 shows the PSRR behavior of the OTA. It is seen that at low frequencies PSRR is 76.8 dB.

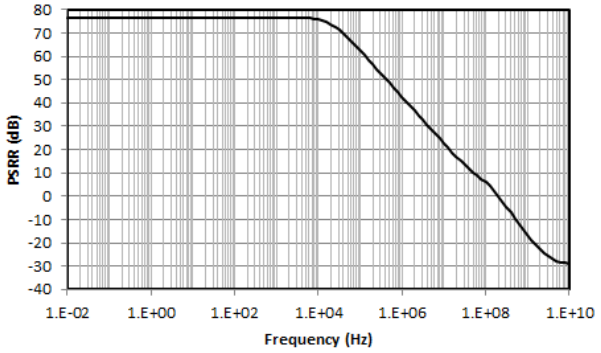


Fig. 11. Magnitude of OTA PSRR as a function of frequency.

The total power consumption of the OTA is found by multiplying the total current supplied by the 1.8V power supply when a 0.9V input is applied. This current is found to be 259.6 μA, which implies a total power consumption of 0.467 mW.

Lastly, a discussion is provided to address differences between the initially calculated values of the OTA specifications and the final realized numbers. Table III shows a summary of this information.

Table III. Summary of hand calculated values of various design specifications versus final simulated values.

		Hand Calculation	Final Simulation
DC small-signal gain		74.9 dB	74.25 dB
Unity gain frequency		90 MHz	101 MHz
Phase margin		67.4°	55°
Power Consumption		0.54 mW	0.467 mW
Settling time	Going up	22 ns	21.4 ns
	Going down	22 ns	32.4 ns
CMRR at DC		76.4 dB	70.35 dB

The differences in unity gain frequency and phase margins were expected. During the initial design by hand it was noted that the unity gain frequency was a little lower than desired, but it was decided to do the final tuning in the simulation phase together with other inevitable discrepancies. These values, together with the settling time are dependent on the locations of the poles and zeroes of the system. During the final design phase the values of R_z and C_c were modified to attain the desired 100 MHz unity gain frequency by sacrificing some phase margin. The settling time difference in the downward step input can be attributed to the fact that the slewing time was underestimated The lower power consumption number in the final design is due to the fact that the reference current was reduced from 50 μA to 12.46 μA while increasing the current mirror ratio up to the allowed limit of 20 in the final design. This allows a reduction in power consumption. The difference in CMRR is due to an under-estimation of g_{ds7} in the hand calculations. M7 operates near the edge of saturation and its g_{ds} is likely to be higher than what is estimated from the technology charts.

IV. Conclusions

The design of a low-power OTA is described in the report. A pole-zero cancellation strategy is used in this design allowing some flexibility in tuning the unity gain frequency, phase margin, and settling time. The specifications provided are met or exceeded. An initial design by hand is done which serves as the starting point for the final simulation based refinement. Differences between the hand calculations and final simulated results are described.

References

[1] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, Analysis and Design of Analog Integrated Circuits, 4th ed. New York: Wiley, 2001.