EE338L Final Project

Design and Simulation of a Low-Power Two-Stage Operational Transconductance Amplifier

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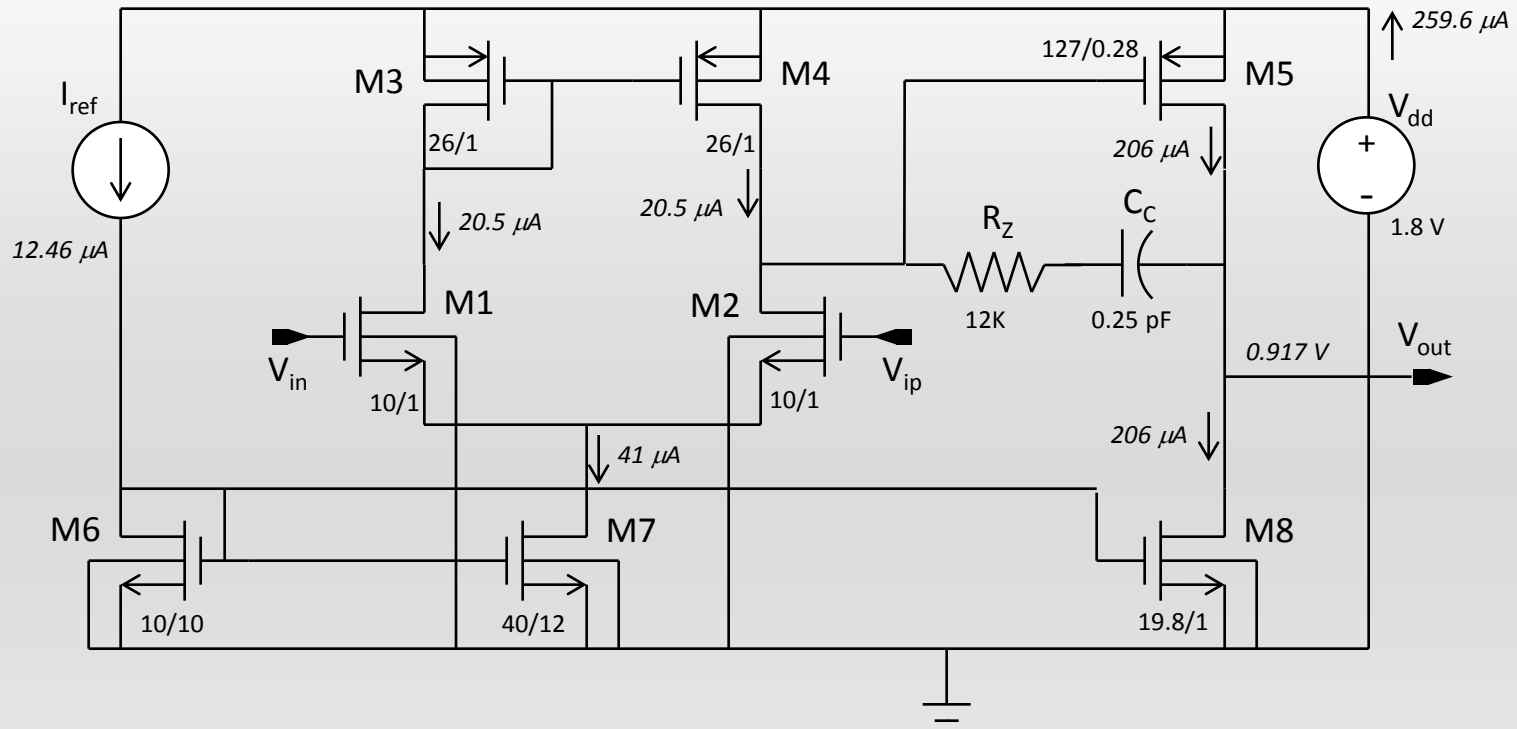
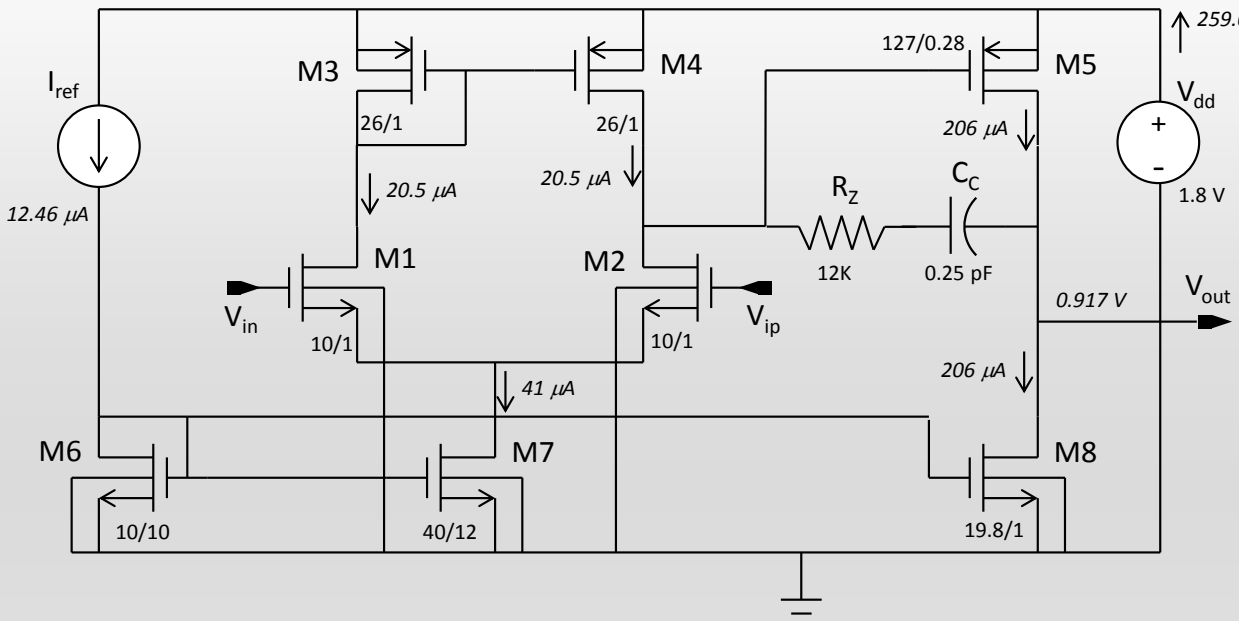
Two Stage OTA Design



- Advantages compared to cascoded or telescopic differential stages
  - Lower power consumption of only 0.467mW
  - Simpler design allows for analytical debugging

- Larger MOSFET length (L = 1um) reduces random mismatch and improves offset

Design Strategy



$$A(s) = A_{v0}\frac{\left(1-\frac{s}{z_1}\right)}{\left(1-\frac{s}{p_1}\right)\left(1-\frac{s}{p_2}\right)\left(1-\frac{s}{p_3}\right)}$$

$$T(s) = \frac{\beta A_{v0}}{\left(1-\frac{s}{p_1}\right)\left(1-\frac{s}{p_2}\right)}$$

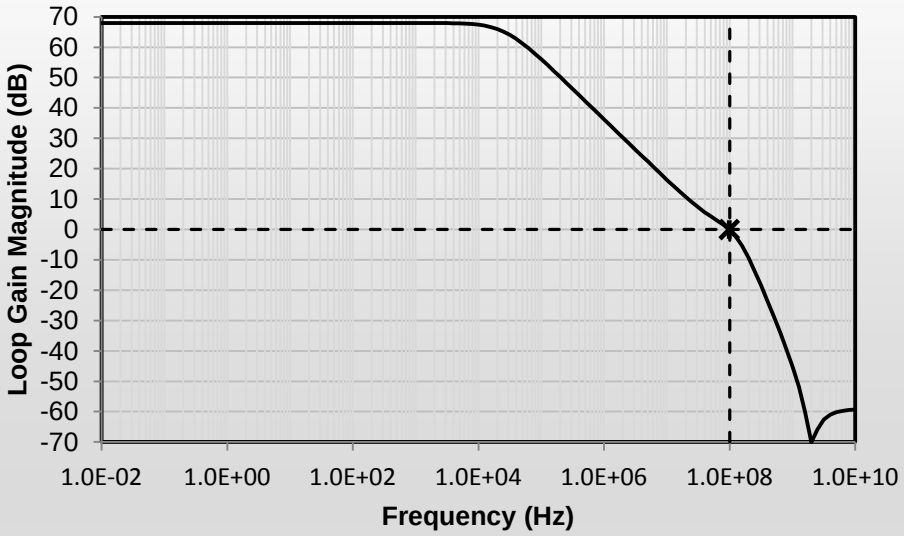
- Circuit elements (sizes, biases, etc.) are chosen such that the zero cancels pole p3
  - Result is a two-pole loop gain expression
  - Manageable analytical expressions for unity gain frequency and phase margin
  - Compensation capacitor Cc results in "pole splitting"
  - Nulling resistor results in LHP zero and allows pole-zero cancellation

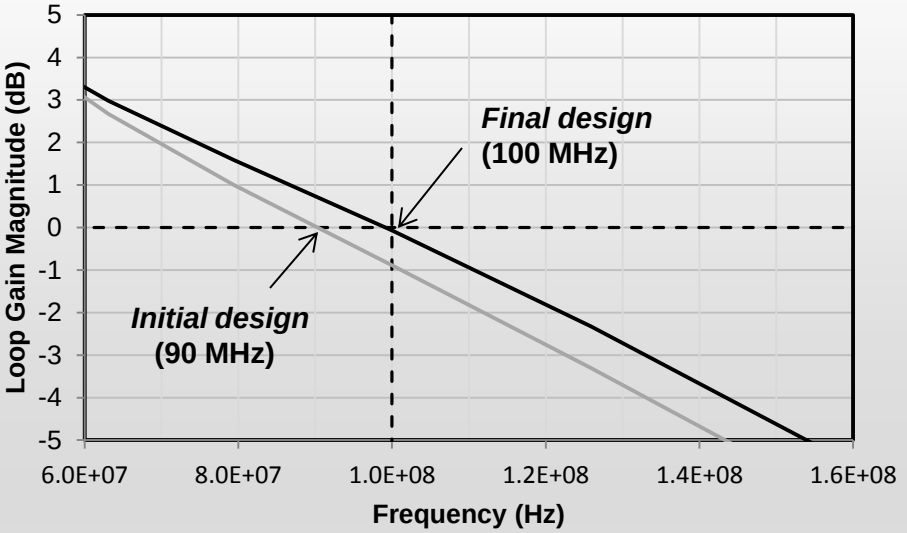
Simulation Results

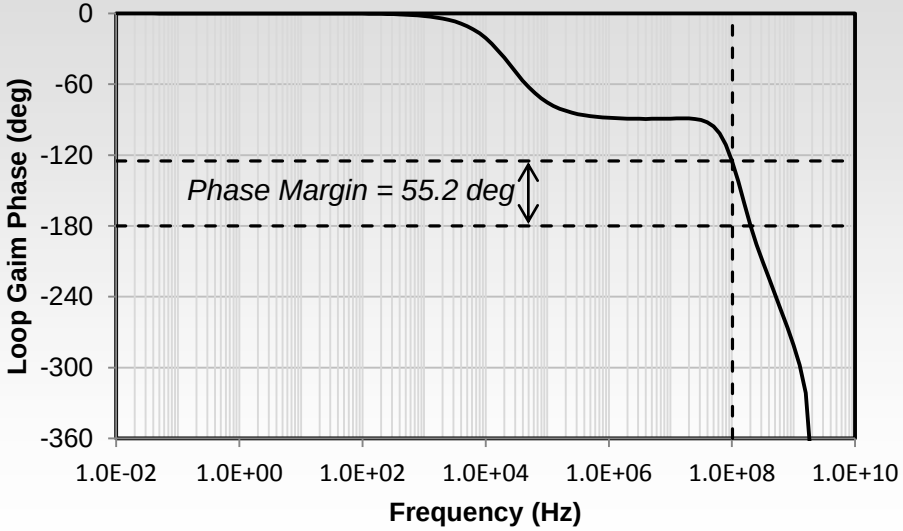
		Specification	From Theory	Final Design
DC small-signal gain		> 70 dB	74.9 dB	74.25 dB
Input-referred offset		< 10 μV	n/a	-1.6 μV
Input V_{cm} range		[0.75, 1.05]	n/a	[0.75, 1.05]
Output swing		[0.3, 1.5]	n/a	[0.275, 1.56]
Unity gain frequency		> 100 MHz	90 MHz	101 MHz
Phase margin		> 45°	67.4°	55°
Power Consumption		< 1 mW	0.54 mW	0.467 mW
Settling time	Up	< 40ns	22 ns	21.4 ns
	Down	< 40ns	22 ns	32.4 ns
CMRR at DC		> 70 dB	76.4 dB	70.35 dB
PSRR at DC		> 70 dB	n/a	76.8 dB

- Paper design completed as first phase of project
- Initial paper design was reasonably close to target (with known exception of ω_u)
- In second phase design was tuned to final targets using Spice
  - Phase margin sacrificed for unity gain frequency
  - Reference current reduced by pushing current mirror ratios to max limits

Adjusting Unity Gain Frequency

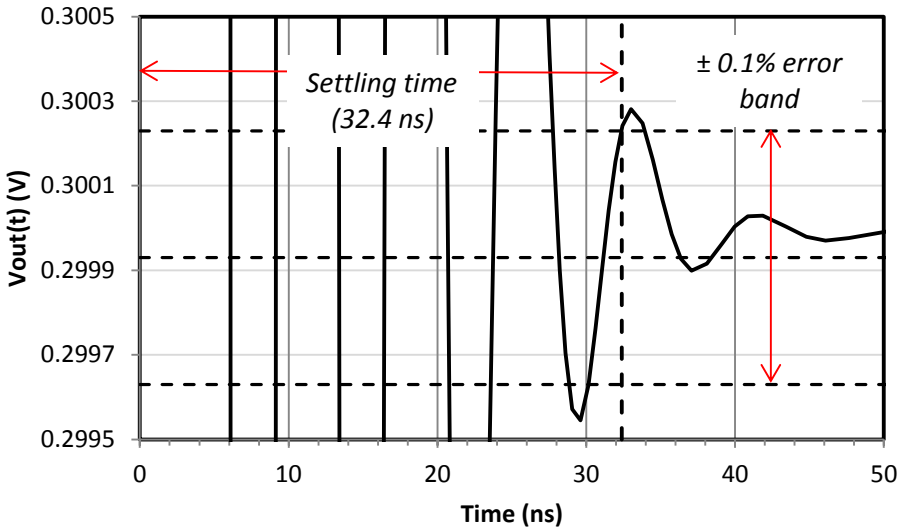


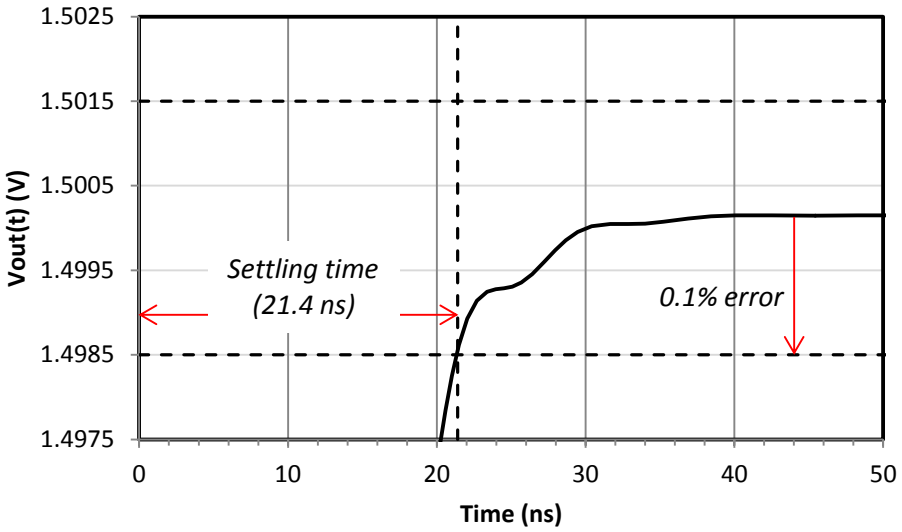




- Loop gain characteristics for initial theoretical design and final design are shown
- Initial design was a little short of target unity gain frequency
  - *Corrected by adjusting Rz*
- Final design met both unity gain frequency and phase margin targets

Settling Time



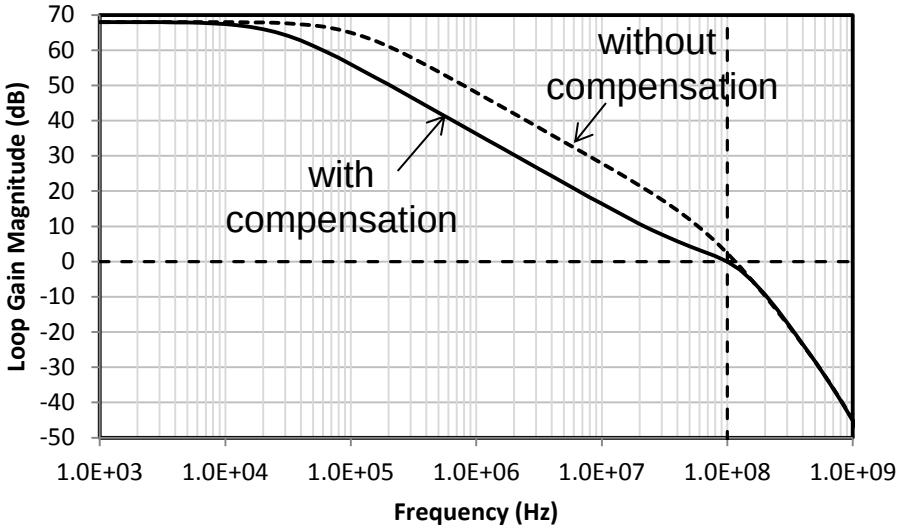


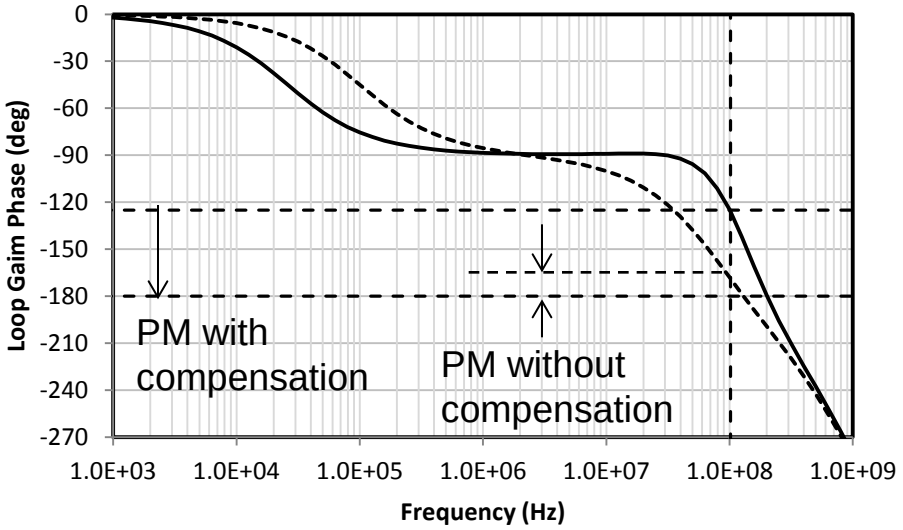
Upward Input Step

Downward Input Step

- Settling time characteristics adequately meet specifications in both directions
- Shows ringing behavior as expected from thoery
  - Frequency of ringing is close to theoretically calculated value
- Upward step input settling time higher in Spice than in theory
  - Probably due to approximations made regarding the various capacitances and assuming the system to be linear

Effect of Compensation Circuit





- Loop gain characteristics for final design are shown with and without the compensation capacitor and nulling resistor
- Not much effect on unity gain frequency (slight zero observable)
- Significant improvement on phase margin with compensation circuit