EE462L – H-Bridge Audio Amplifier - PART 1: PWM Controller Circuit

Team 255 – Rounok Joardar, Jonathan Lew

Spring, 2015

Lab Overview

The H-Bridge Converter is an all-purpose power converter that can handle DC-DC, DC-AC, AC-DC, and AC-AC conversion. Most frequently the H-Bridge is used as an inverter, taking a DC input and transforming that to an AC output. Through the utilization of four power electronics switches configured in an "H" pattern, it can create a nearly sinusoidal output waveform. The H-bridge achieves this through a process called pulse width modulation. Pulse width modulation is a process where a control signal is compared to a known periodic signal, such as a square or triangle wave, and when the control signal is higher than the known periodic signal, the output waveform is high. When the control signal is lower than the known periodic signal, the output waveform is low. With a sinusoidal control signal, pulse width modulation results in square waves with different widths that are proportional to the sinusoidal control signal's amplitude. In order to achieve pulse width modulation, a known periodic signal must be created and used to compare against the control signal. The H-bridge controller circuit built in this lab provides that function and other functions such as the H-bridge switching controls.

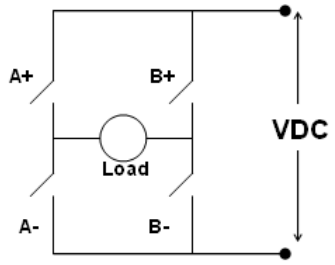


Fig. 1. H-Bridge inverter/amplifier circuit made from four MOSFET switches. Freewheeling diodes are not shown. [1]

H-Bridge Gate Control Circuit

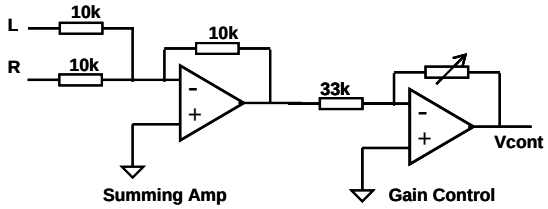
The purpose of this lab is to build and test the gate control circuit for a H-Bridge inverter/amplifier. This circuit is used to generate the gate signals for the four mosfet switches of Fig. 1. The A+ and A- mosfets are switched with a signal VA and its inverse. When VA is high A+ is on, and A- is off. Similarly, the B+ and B- mosfets are switched using a signal VB and its inverse.

The signal VA is the output generated by feeding a low frequency control signal Vcont and a high frequency triangular wave Vtri into a comparator. It is important to note that the frequency of Vtri needs to be much greater than the frequency of Vcont for proper filtering of the H-Bridge output signal. When used as an inverter, the frequency of Vcont is the desired frequency of the ac output of the H-Bridge inverter. This is typically 60 Hz. The output of the comparator used in this circuit switches between +12V and -12V.

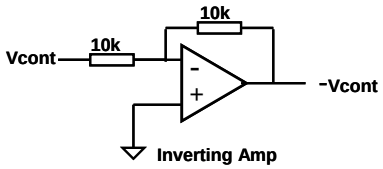
The signal VB is similarly generated by feeding the negative -Vcont, of the control signal, and the same triangular wave to a comparator.

Fig. 1 shows a schematic of the circuit used to generate Vcont from a stereo signal. The left and righ channel signals are summed using a op amp summing amplifier. The summed signal is then attenuated or amplified further using a second op amp. The negative of Vcont (i.e. -Vcont) is generated using an op amp in inverting amplifier configuration with gain of 1.

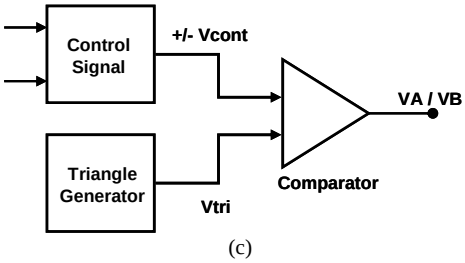
The triangular wave is generated by using a NTE864 precision waveform generator chip. The frequency of the triangular wave is determined by a timing capacitor Cf. In this circuit a Cf of 1.5nF was used, which produced a triangular wave of frequency 139 kHz.



(a)



(b)



(c)

Figure. 2. (a) Schematic of circuit used to generate the control signal Vcont for the H-Bridge gate controller. (b) Schematic of circuit used to generate the negative image of Vcont. (c) Block diagram of gate drive circuit.

H-Bridge Controller Measurements

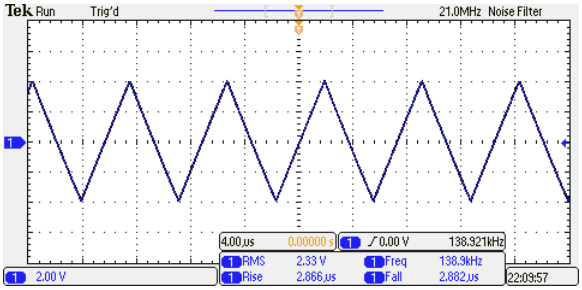


Figure. 3 Measured triangular signal Vtri. The frequency of the signal is 139 kHz.

Fig. 3 shows the measured triangular wave Vtri with a 1.5nF timing capacitor. The skewness pot of the waveform generator chip is adjusted such that the rise and fall times of Vtri are equal to the first decimal place. The ZeroDCOffset pot on the PCB is also adjusted such that the dc value of Vtri is 1 mV.

For purposes of testing, the control signal is obtained from an ac wall wart. This generates a 60Hz signal which is fed into the "left" channel of the control circuit. By adjusting the gain potentiometer shown in Fig. 2 the RMS value of Vcont is set to be 2.01V. Fig. 4 shows the measured Vcont and -Vcont waveforms.

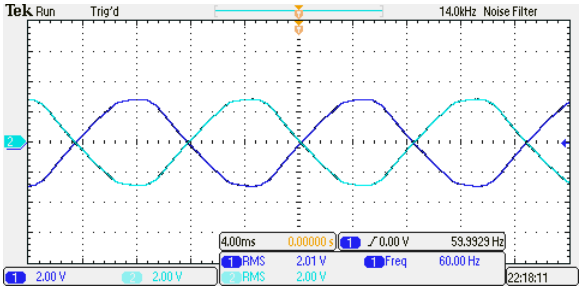


Figure 4. Measured control signals Vcont and -Vcont obtained from wall wart output. The frequency is 60Hz and the rms value is 2.01V.

As described previously, the H-Bridge gate control signals VA and VB are obtained, respectively, by feeding Vcont and Vtri and -Vcont and Vtri to a comparator.

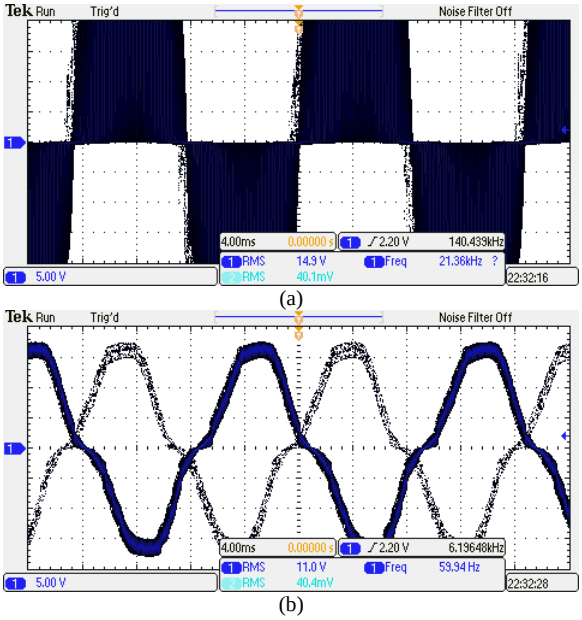
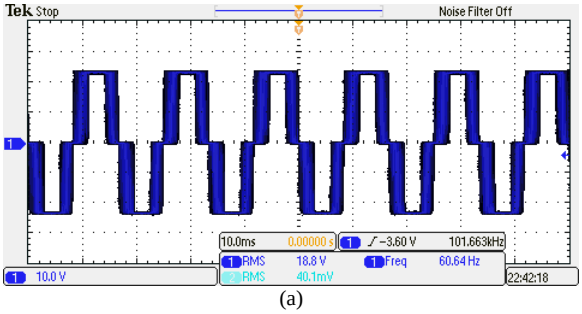


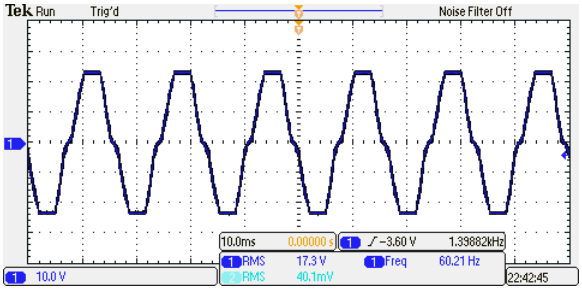
Figure 5. (a) Unfiltered waveform VAB and (b) filtered version of waveform VAB. The fundamental frequency is about 60 Hz.

Fig. 5(a) shows the resultant VAB (=VA-VB) signal. It is impossible to discern the PWM nature of the waveform at this timescale due to the very large difference in the frequencies of Vtri and Vcont, but it is evident that the signal has a fundamental frequency of about 60 Hz. Fig. 5(b) is the same signal passed through the scope filter. With the higher harmonics removed the signal begins to resemble Vcont.

Next, the effect of increasing the amplitude of Vcont to the point where it exceeds the amplitude of Vtri is examined. Fig. 6 shows the measured unfiltered and filtered VAB waveforms under these overmodulated conditions ($m_a > 1$). As expected from theory, the peaks of VAB are clipped and a shoulder appears near the zero-crossings.



(a)



(b)

Fig. 6. (a) Unfiltered waveform VAB under overmodulation conditions and (b) filtered version.

In order to examine the frequency content of VAB an FFT of the VAB waveform was captured in the linear modulation region. Fig. 7 shows the resultant spectrum.

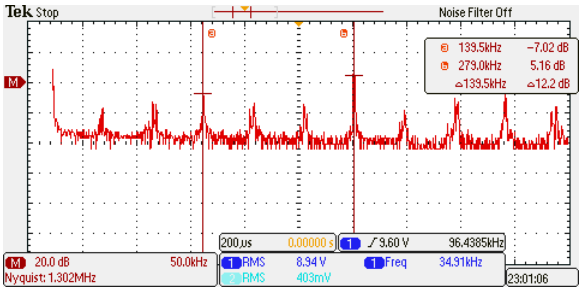
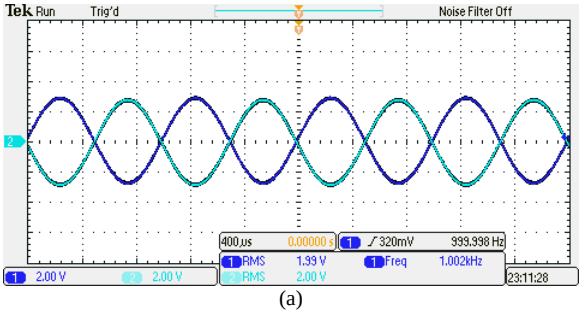


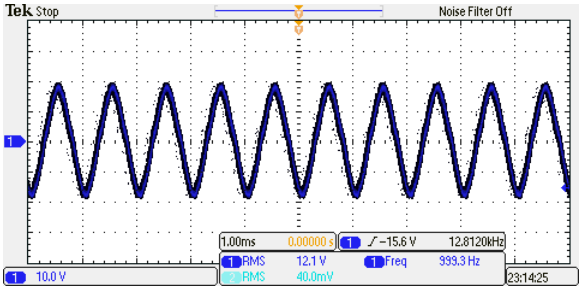
Figure 7. FFT of VAB signal in the linear region.

It can be seen from Fig. 7 that the non-ideal 139.5 kHz peak is about 12 dB below the first ideal peak at 279 kHz. That corresponds to a factor of about 4.

Lastly, the effect of increasing the frequency of the control signal Vcont is examined. Fig. 8 shows a 1 kHz Vcont control signal and the corresponding filtered VAB output waveform. Fig. 9 shows the same signals at a frequency of 10 kHZ.

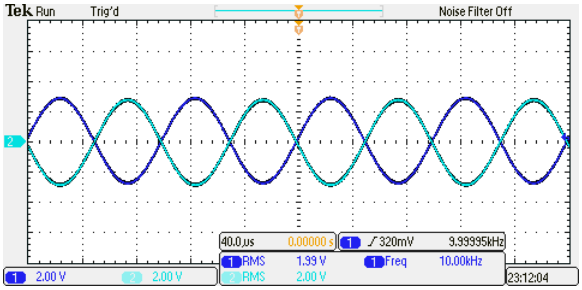


(a)

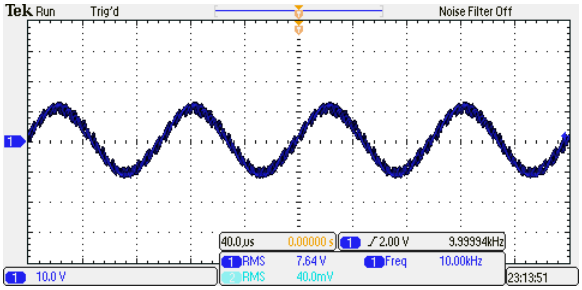


(b)

Figure 8. Vcont and VAB waveforms taken at 1 kHz frequency.



(a)



(b)

Figure 9. Vcont and VAB waveforms taken at 10 kHz frequency.

The output signal VAB at these frequencies are reasonably similar to the respective control signals. At 10 kHz there is some evidence of high frequency harmonics even in the time domain data of Fig. 9(b). This could be due to mixing of Vcont and Vtri since their frequencies are now less separated than in the other cases and also possibly due to the oscilloscope filter not having a sharp enough cut-off.

Conclusions

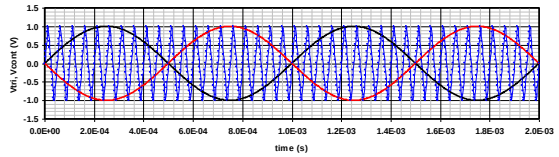
The H-Bridge controller circuit provides all the necessary components for the H-bridge to properly function, except for the MOSFETs themselves and the direct MOSFET support circuitry. The controller circuit takes the input control signal, inverts it and uses both the original and inverted signal compared to a triangle signal to provide the pulse width modulation for the H-bridge. These pulses directly correspond to certain MOSFETs being turned on or off will provide the load with a sinusoidal like signal

with harmonics in high frequencies that can be eliminated by using a low pass filter. Without pulse width modulation, the harmonics would not be pushed out to higher frequencies and it would be difficult to filter out the harmonics without losing the fundamental signal.

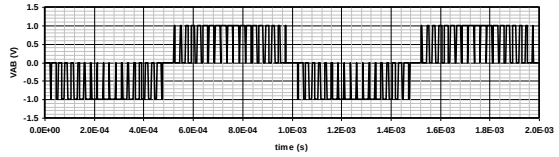
APPENDIX

In order to better study the generation of the complex PWM gate drive signals and the properties of the H-Bridge output signal, an Excel spreadsheet was constructed. By changing the inputs in this spreadsheet the ideal theoretical relations between the various signals can be observed more closely.

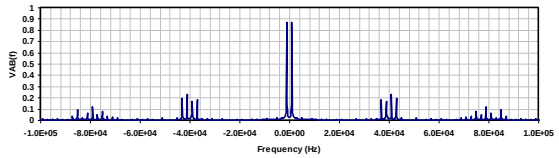
Since Excel does not have a built-in triangular function, Vtri was constructed by summing the first 9 sine wave harmonics of a periodic triangular signal.



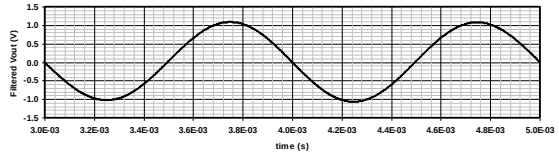
(a)



(b)



(c)



(d)

Figure 10. Various H-Bridge waveforms as simulated in Excel. (a) The triangular wave (20kHz) and the sinusoidal control signals (1 kHz). (b) The difference VAB between the comparator outputs from the positive and negative control signals. (c) The double-sided FFT of VAB. (d) Inverse FFT after passing VAB through a low-pass filter with 1.1kHz cut-off frequency.

Fig. 10 shows the various simulated waveforms. For the results shown a frequency of 20 kHz was used for the triangular wave and 1 kHz for the control signal. Equal amplitudes were used for both triangular and control voltage signals (i.e. modulation index = 1). The simulation was performed till 8.2 ms with a timestep of 2 μs. Excel's built-in Fourier Analysis tool was used to observe the harmonics of VAB, as shown in Fig. 10(c). A 2-sided FFT is shown. As expected from theory, there is a strong signal at 1 kHz which is the frequency of Vcont in this simulation, plus harmonic clusters around even multiples of the triangular wave frequency.

The frequency domain signal was passed through an ideal low-pass filter with a cut-off frequency of 1.1 kHz. Phase of the filter transfer function was ignored to keep the simulation simple. Taking the inverse FFT of the filtered signal results in a very clean output that is a replica of the control sine wave in time domain, as shown in Fig. 10(d). By increasing the DC voltage supply to a H-Bridge the amplitude of VAB can be increased, which will result in an amplified version of the control signal at the output.

EE462L – H-Bridge Audio Amplifier - PART 2: Power Stage Circuit

Team 255 – Rounok Joardar, Jonathan Lew

Spring, 2015

Lab Overview

This lab is a continuation of the previous work on building and testing an H-Bridge power electronics circuit. Previously, we had only constructed the PWM control board for the H-Bridge circuit, but we now build the actual H-Bridge circuit itself. We attached the previously constructed PWM control board to the H-Bridge power circuit and use the two together to invert a 35-40VDC signal to a 60Hz AC waveform. A simplified figure of what the H-Bridge power circuit looks like can be seen in Fig. 1. The output from the H-Bridge is measured across a 5Ω load at different DC input voltages and using two separate triangle comparator frequencies.

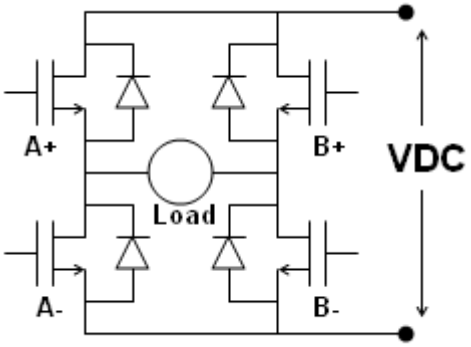


Fig. 1. H-Bridge inverter circuit made from four MOSFET switches. Freewheeling diodes are internal to the mosfets.

H-Bridge Gate Voltage Generation

The PWM output signals generated by the controller circuit constructed in the previous lab cannot be directly connected to the gates of the H-Bridge mosfets. The gate signals for the A+ and B+ mosfets (high side mosfets) need to be level shifted so that they are referenced to their source voltages. Also "dead time" needs to be added between the high side and low side gate signals to prevent the high side and low side mosfets from being on simultaneously (shoot through).

Two half-bridge driver ICs (International Rectifier part 21844) are used to process the H-Bridge gate drive signals. A simplified schematic of how the PWM signal, gate driver circuit and H-Bridge are hooked up is shown in Fig. 2.

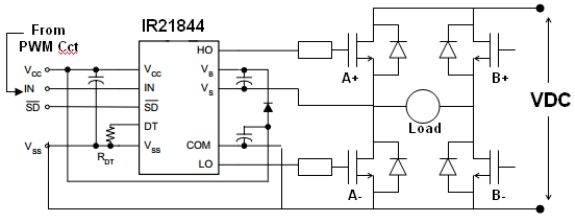


Fig. 2. Schematic showing gate drive signal generation for H-Bridge inverter circuit using IR21844 half bridge gate driver IC. Connections to only the gates of left half of bridge are shown. Right half bridge is connected to an identical circuit.

H-Bridge Measurements

This section describes the various measurements made after assembling the H-Bridge power stage PCB and connecting it to the controller PCB from the last lab.

Fig. 3 shows the measured signal at the gate of one of the mosfets with no load connected across the H-Bridge output. The control voltage on the PWM circuit is set to zero in this case. As expected, the waveform is a square wave (~ 50% duty cycle) because it is generated by comparing a symmetrical triangular wave with zero volts. The frequency of this signal is 139.4 kHz which is the frequency of Vtri in the PWM circuit. The height of the pulses is about 10V.

Fig. 4 shows the same gate signal with higher Vcont. Again, as expected, the pulse width narrows as Vcont increases because the triangular voltage Vtri is compared against a higher level. Unfortunately, there is a lot of jitter in the scope screen capture, possibly due to the effect of the lower frequency of Vcont.

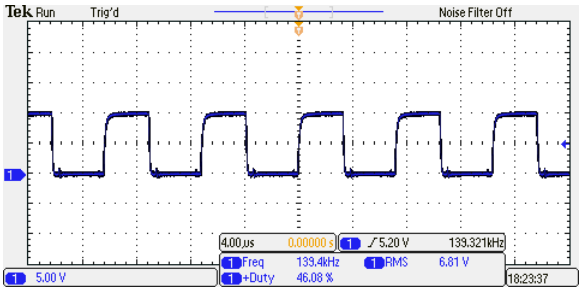


Figure. 3 Measured signal at mosfet gate with Vcont = 0 in the PWM controller circuit.

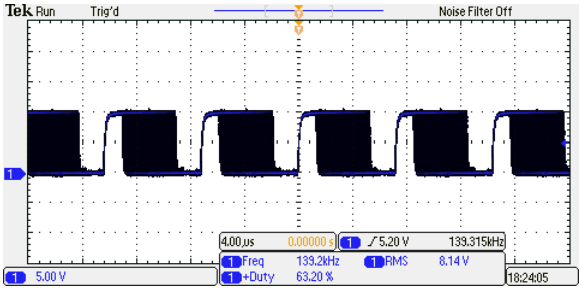


Figure. 4 Measured signal at mosfet gate with Vcont increased above in the PWM controller circuit. There is a lot of jitter in the waveform.

Next, a 5Ω load is attached across the H-Bridge output and its dc voltage is increased to 10V. The resulting voltage waveform at the inverter output is shown in Fig. 5. The frequency of the output signal is 60Hz, duty cycle is 49.42% (i.e. almost symmetric) and its peak to peak amplitude is about 15V. The RMS voltage as reported by the scope is 4.9V. A multimeter reading of the RMS output voltage was 4.85V which is very close to the scope estimate. The corresponding power dissipation is 4.8W.

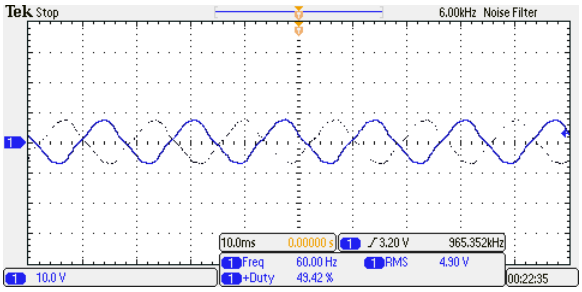


Figure 5. H-Bridge inverter output waveform with 5Ω load and 10V dc input. Frequency of inverter output is 60Hz and peak-peak amplitude is about 15V.

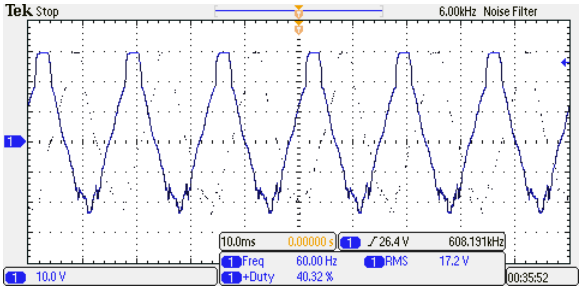


Figure 6. H-Bridge inverter output waveform with 5Ω load and 35V dc input. Frequency of inverter output is 60Hz and peak-peak amplitude is about 54V.

Fig. 6 shows the same H-Bridge inverter output waveform with but with the dc voltage increased to 35V. There is significant deterioration in the shape of the waveform possibly due to parasitic inductance in the wires and load resistor. The frequency of the output waveform is still 60Hz and the RMS voltage is 17.2V as reported by the scope. This corresponds to a power dissipation of 59.2W. On a multimeter the RMS reading is 19.73V which corresponds to a somewhat larger power dissipation of 77.9W. The mosfet heat sinks felt slightly warm to touch.

Next, in order to improve the shape of the output voltage waveform at high dc input, the carrier frequency in the PWM controller was reduced by increasing the CF capacitor in the controller circuit to 4.7nF. This reduces the frequency of Vtri to 44 khZ. It is expected that at lower frequency some of the parasitic effects would be less leading to a cleaner waveform. Results are as shown in Fig. 7. The waveform is definitely cleaner compared to Fig. 6. The frequency is 60Hz, peak to peak amplitude is about 52V, and RMS voltage reported by the scope is 16.8V which is a bit lower than in the previous case. This RMS voltage corresponds to a power dissipation of 56.4W in the 5Ω resistor. Interestingly, the RMS reading on a multimeter increased to 22.3V in this case which implies a power dissipation of 99.5W in the 5Ω load resistor.

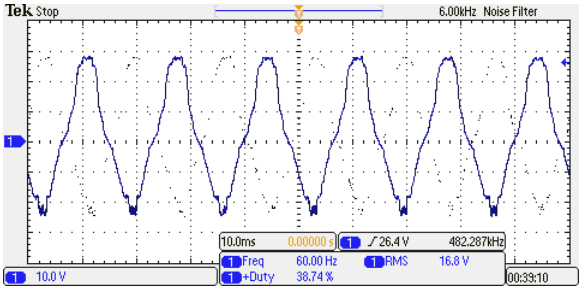


Figure 7. H-Bridge inverter output waveform with 5Ω load and 35V dc input. Frequency of inverter output is 60Hz and peak-peak amplitude is about 52V.

Conclusions

This is the first time we see the full H-bridge circuit in action. Previously, we had only seen the control circuit, which takes care of the pulse width modulation and creates an inverse control signal to control both legs of the H-bridge. We see that at a low input voltage the output of the H-bridge is very sinusoidal, but when raising the DC input voltage, inductance in the 5Ω power resistor seriously distorts the output signal. One way to remedy this is to reduce the switching events by lowering the frequency of Vtri. A slight improvement in the output waveform can be seen by lowering the frequency of Vtri via the 4.7nF CF capacitor, but not enough to offset the inductance of the load.

EE462L – H-Bridge Audio Amplifier - PART 3: Audio Amplifier

Team 255 – Rounok Joardar, Jonathan Lew

Spring, 2015

Lab Overview

This lab is a further extension of the previous work on building and testing a H-Bridge circuit. In this lab an audio source is used as th

e PWM control signal and the amplification level is changed by adjusting the DC voltage of the H-Bridge [1]. A block diagram is shown in Fig. 1.

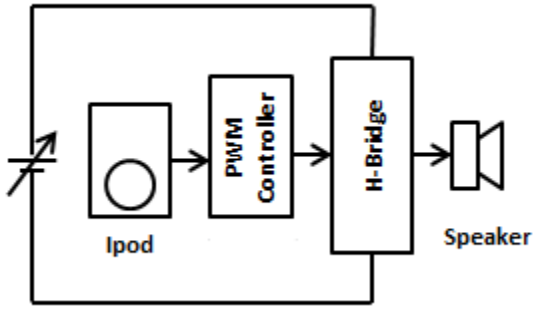


Figure 1. Block diagram of H-Bridge circuit based audio amplifier.

Modulation Index Measurements

In a H-Bridge amplifier it is important to set the modulation index m_a close to 1. If m_a is much less than 1 then the fundamental component in the H-Bridge output, which is the main signal of interest, will be weak. If m_a is much bigger than 1 the output signal will be clipped and distorted. This section describes various methods to check the modulation index m_a.

In the first method, the PWM controller circuit is first adjusted to set the carrier signal Vtri to be around 137 kHz (using a 1.5nF C_F capacitor) and to ensure the triangular wave is symmetric. Then a 4V, 100 Hz sinusoidal control signal Vcont is applied from a signal generator. The two signals are observed simultaneously on an oscilloscope and the amplitude of the Vcont wave is adjusted to make it visually equal to the amplitude of Vtri. Fig. 3 shows the resulting waveforms. The heights of the two waveforms are about the same. The scope readouts are 8.40V and 8.32V for Vtri and Vcont, respectively. This implies a modulation index of 0.99. Additionally, the frequency ratio m_f from the scope readouts is 140.4kHz/99.97Hz or 1404.42.

In the second approach, the PWM signal VA-VB was observed on the oscilloscope. Results are as shown in Fig. 3. It is seen that there is a "gap" in the middle which indicates some amount of overmodulation.

In the third approach, the same VA-VB waveform is examined, but a filtered view is used. Results are as shown in Fig. 4. There is a small amount of clipping at the tops of the wave, indicating a small amount of overmodulation.

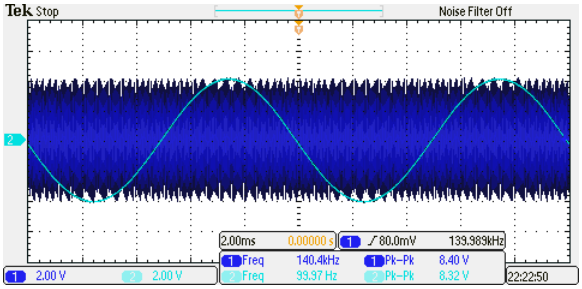


Figure. 2 Measured Vcont and Vtri signals showing a modulation index very close to 1.

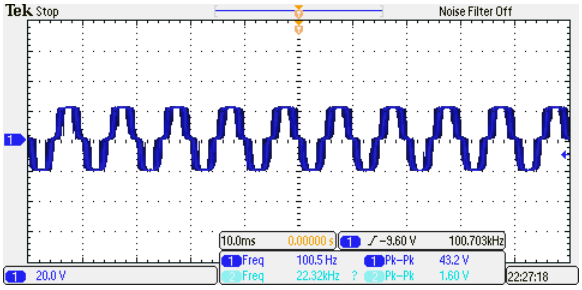


Figure. 3 Measured PWM signal VA-VB, unfiltered.

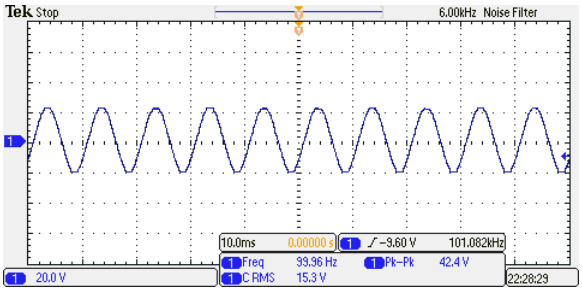


Figure 4. Measured PWM signal VA-VB, filtered.

Based on the above results it appears that the second method of using unfiltered (VA-VB) is the best method to achieve a modulation index of 1. A suitable procedure would be to keep increasing the amplitude of Vcont from a small value till as "gap" just appears in the unfiltered view and then pull back

a bit to close the gap. Fig. 5 shows such a waveform of (VA – VB) which is at the edge of $m_a = 1$..

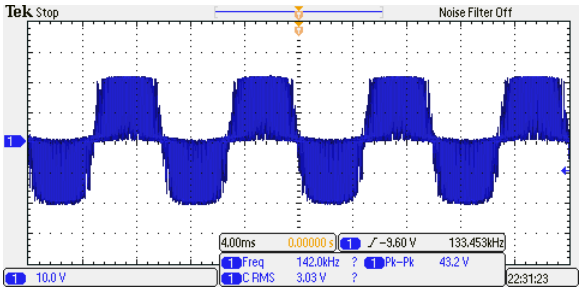


Figure 5. Unfiltered VA-VB output at the edge of over-modulation..

H-Bridge Output and Efficiency Measurements

Next, a nominal 10 ohm power resistor is connected to the H-Bridge output. The exact value of this resistor, as measured on a multimeter, is 10.5 ohms. The AC supply to the DBR powering the H-Bridge is adjusted to about 28V. The modulation index is adjusted to 1 and a 100Hz sine wave with 4V amplitude is used as Vcont. Fig. 6 shows the resulting output signal. The lower sine wave is the 100 Hz Vcont signal. Its rms is 2.67V compared to a theoretically expected value of $4/\sqrt{2} = 2.83$V. The upper waveform is the filtered H-Bridge output. Its frequency is practically the same as the frequency of Vcont, i.e. 100Hz, and its rms voltage is 9.03V. Careful observation shows a slight distortion around the zero crossing points. This is due to the dead time introduced by the gate drive circuit in order to prevent the possibility of shoot through where both high side and low side mosfets of the H-Bridge are conducting at the same time.

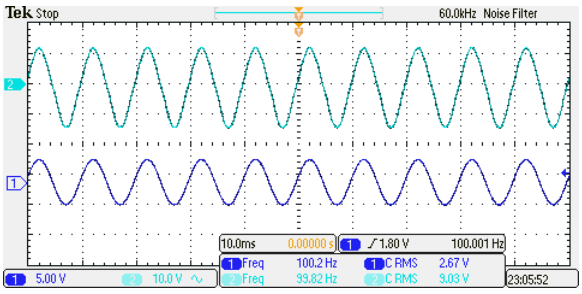


Figure 6. Measured waveforms of Vcont and H-Bridge output.

Using a multimeter, the dc voltage at the H-Bridge output is measured. It is found to be 23 mV which is negligibly small.

In order to estimate the efficiency of the H-Bridge amplifier, the input DC voltage and current are measured. These are found to be 34.61V and 1.36A, respectively. Thus, the input power is 47.07W. On the output side, the ac voltage is measured to be 19.49V. Since the load resistor is 10.5 ohms, the output power is 36.18W. This implies an efficiency of 76.9%. This is comparable to the efficiencies measured in the dc-dc converter experiments.

H-Bridge THD Measurements

Next, the THD of the H-Bridge amplifier is estimated from the FFTs of the output waveform for control signal frequencies of 100 Hz, 1 kHz, and 5 kHz. Fig. 7 shows the FFT of the H-Bridge output with a control signal frequency of 100 Hz. The fundamental output is 20dB while the third harmonic is at -7.2dB. Ignoring the contributions of higher harmonics the resulting THD is 4.37%.

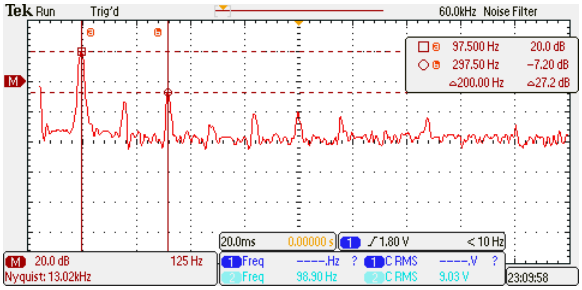


Figure 7. FFT of H-Bridge output with 100Hz control signal..

Fig. 8 shows the FFT of the H-Bridge output with a control signal frequency of 1 kHz. The fundamental output is 16.8dB while the third harmonic is at -3.2dB. Again, ignoring the contributions of higher harmonics the resulting THD is 10%.

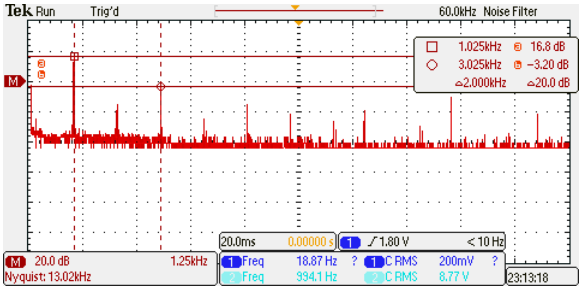


Figure 8. FFT of H-Bridge output with 1kHz control signal..

Fig. 9 shows the FFT of the H-Bridge output with a control signal frequency of 5 kHz. The fundamental output is 20dB while the second harmonic is at 3.2dB and the third harmonic is at -6dB. Again, ignoring the contributions of higher harmonics the resulting THD is 14.5%.

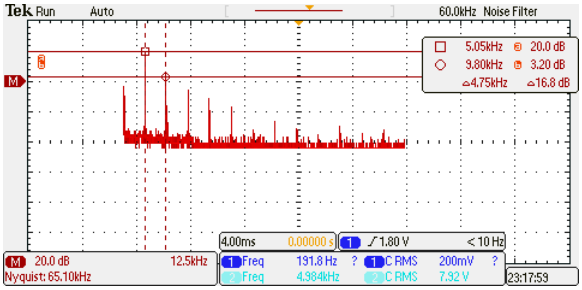


Figure 9. FFT of H-Bridge output with 5 kHz control signal..

Attempts to improve the THD at higher frequencies by lowering fTri (frequenct of the triangular signal) were not very successful. This is probably because it reduces the separation between the harmonics of the control signal and fTri.

Audio Amplifier Measurements

This section describes measurements done with an actual music source feeding into the Vcont port of the H-Bridge amp, as hown in Fig. 1. By adjusting the volume control of the audio source and the gain potentiometer of the controller circuit, the modulation index m_a is first set to about 1. Fig. 10 shows the resulting comparison of the audio signal and Vtri. The amplitudes of both can be seen to be about the same.

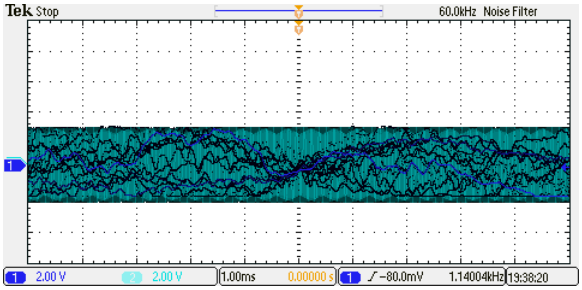
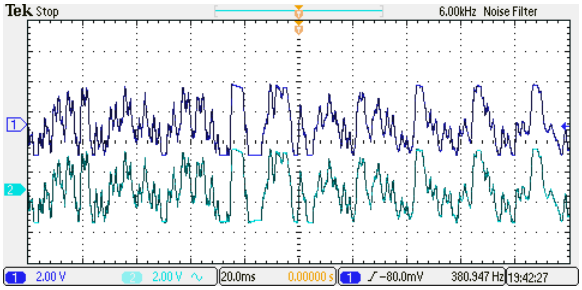
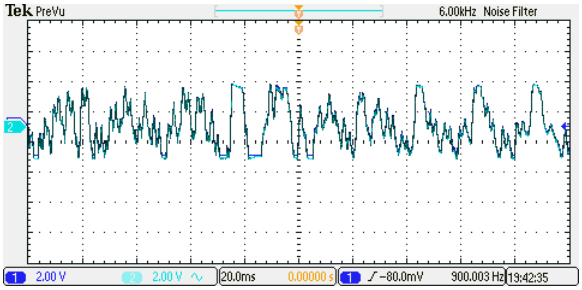


Figure 10. Time domain waveforms of the audio signal and carrier signal (Vtri), showing a modulation index very close to 1.

Lastly, with the H-Bridge powered up, the input and output signals were measured simultaneously on the oscilloscope. Fig. 11 shows the comparison. It is seen that the input and output signals are very similar with a few areas of clipping visible in this passage. The noise filter threshold had to be set at 6 kHz to capture a clean signal although it was recommended to keep this threshold above 20 kHz to allow the entire audible spectrum to pass.



(a)



(b)

Figure 11. Time domain waveforms of the input audio signal and H-Bridge output signal. In (a) the plots are separated, in (b) they are overlayed to show similarity. Probe 1 = input, probe 2 = output.

Conclusions

This lab shows that the H-Bridge we have built and tested previously can function as a decent audio amplifier for those non-audiophiles. The input audio signal and output audio signal after amplification are very similar, however the amplified signal is not an exact replica of the input signal and if the input voltage to the H-bridge is raised too high, the amplified audio signal can become distorted and clip at its peaks.

EE462L – DC-DC Buck Converter

Team 255 – Rounok Joardar, Jonathan Lew

Spring, 2015

Circuit/Lab Overview

The purpose of the Buck converter circuit is to take a DC input voltage, and reduce the input to a lower DC voltage to power a load. A practical application of a Buck converter would be to transform DC voltage from a solar panel to a lower voltage to power equipment. A figure of the Buck converter can be seen below. An idealized Buck converter assumes that Vin is ripple free, the Capacitor C is large enough so that Vout has a ripple of less than 5%, and that the circuit is assumed to be lossless. Assuming Vout is ripple free, Iout is also ripple free. The Buck converter also has two modes, continuous conduction mode(CCM) and discontinuous conduction mode(DCM). In CCM the circuit has two states, with the switch open and switch closed. When the switch is closed, the diode is reverse biased and open, and the inductor is charging. When the switch is open, due to the properties of inductors, the inductor current continuous to circulate through the diode and the diode is forward biased as the inductor discharges. DCM refers to whenever the inductor current reaches zero. When the switch is open, this causes the capacitor to try to reverse the current through the inductor. However this is stopped by the freewheeling diode, and until the switch is closed again, the capacitor provides all power to the load.

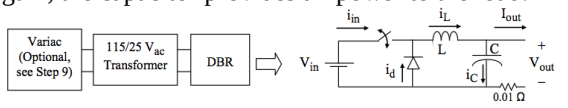
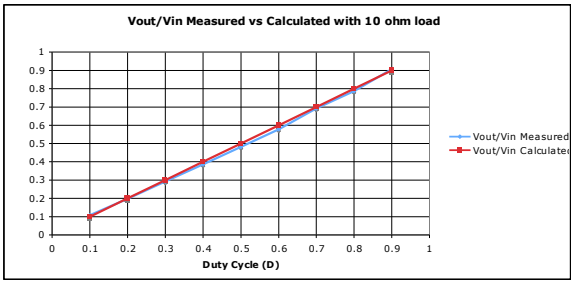
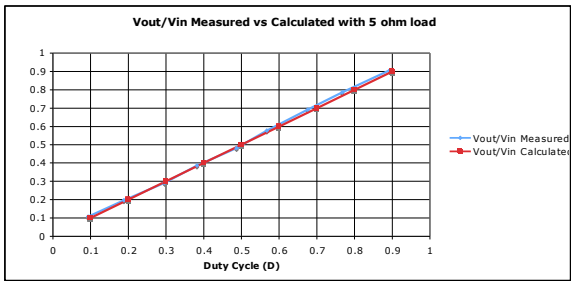


Figure 1: Buck Converter Schematic [1]

Circuit Testing



(a)



(b)

Figure. 2. Measured and theoretical variation of Vout/Vim of a Buck converter as a function of duty factor D with (a) a 10 ohm load, and (b) a 5 ohm load.

Fig. 2. shows the ratio Vout/Vin of the Buck converter as a function of the duty cycle of the mosfet gate voltage for a 10 ohm and a 5 ohm load. Both measured and theoretically calculated values are shown. The measured Vout/Vin ratio overlaps with the expected result with both the 10Ω and 5Ω loads.

Table 1. Measured input currents, voltages, and power consumption of the Buck converte circuit.

	Iin	Iout	Vin	Vout	Pin	Pout	Efficiency
10Ω	3.44A	3.15A	33.2V	30.12V	114.2W	94.9W	83%
5Ω	6.49A	5.89A	32.21V	28.78V	209.04W	169.5W	81%

Table 1 shows a summary of the measured average input and output currents, voltages, and power of the Buck converter circuit at a duty cycle of 0.9. By taking the ratio of output to input power it is found that the efficiency of this converter is slightly above 80%.

Next, the rms values of the inductor and capacitor currents are computed based on theoretical approach. For the inductor, the following equations hold [1].

$$i_{L,avg} = I_{out}, \tag{1}$$

$$\Delta I = \frac{V_{in} - V_{out}}{L} DT = \frac{V_{in}(1-D)}{Lf}, \tag{2}$$

$$I_{rms}^2 = I_{avg}^2 + \frac{1}{12}(\Delta I)^2 \tag{3}$$

Using f = 50 kHz, D = 0.9, Vin = 32.2V, L = 100 μH, gives 5.892A for the inductor rms current. The ΔI term ends up being so small that it falls out of the equation leaving Irms = Iavg = Iout. The capacitor rms current is simply the rms of ΔI. Since ΔI is triangular, its rms is ΔI/(2√3). Using (2) this results in a value of 0.167A for the capacitor rms current.

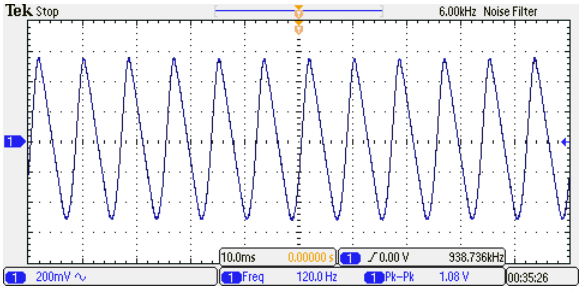


Figure 3: Peak-to-Peak Ripple Voltage, Vin (5 **Ω** Load, D = 0.9, f = 15-20 kHz)

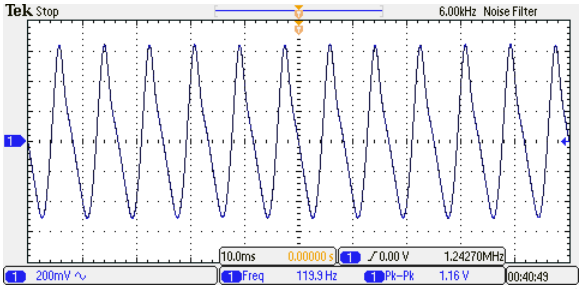


Figure 4: Peak-to-Peak Ripple Voltage, Vout (5 **Ω** Load, D = 0.9, f = 15-20 kHz)

Fig. 3 and Fig. 4 show the measured 120 Hz ripple on the input and output voltages. The measurements were done at a switching frequency of about 16.5 kHz with a 0.9 duty cycle. The peak-peak 120 Hz ripple is 1.08V on the input and 1.16V on the output. This ripple waveform originates from the diode bridge rectifier (DBR). The ripple frequency is 120 Hz, not 60 Hz, because of the DBR is a full wave rectifier in which the ripple frequency is double the input sin wave frequency because it is fully rectified (basically it makes $|V\sin(\omega t)|$). In order to calculate the rms ripple voltages we assume the 120 Hz ripple to be triangular in shape. Utilizing equation 4 [1], the results are listed below in Table 2. Measured data, obtained using an ac multimeter are also shown.

$$V_{rms} = \frac{V_{pp}}{2\sqrt{3}} \qquad (4)$$

Table 2. Calculated and measured rms voltages

	Calculated	Measured
Vrms_in	0.31	0.42
Vrms_out	0.33	0.45

There seems to be a 0.1 offset when measuring Vrms with a multimeter. This is likely because the signals are not purely triangular or a error in the multimeter reading due to lack of calibration.

Next the high frequency ripple due to the gate switching is examined by zooming in on the Vout transient. Fig. 5 shows the measured ripple waveform. The peak-peak ripple is measured as 154 mV at a frequency of 16.56 kHz.

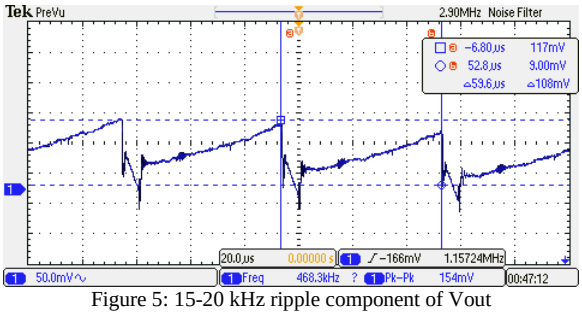


Figure 5: 15-20 kHz ripple component of Vout

Theoretically, the worst case Vpp ripple is given by [1]:

$$V_{pp,ripple} = \frac{I_{out}}{4Cf} \qquad (5)$$

From equation (5) the theoretically calculated Vpp = 59mV in the worst case. The measured peak-peak ripple is much higher. There are a few "spikes" in the measured zvout waveform. If these are ignored, the peak-peak measured ripple can be estimated to be about 90 mV, which is still significantly higher than the worst case estimate. The difference could be due to the capacitor's effective series resistance which would add more ripple voltage because it would be multiplied by the ripple current originating from the inductor.

The rms voltages corresponding to the measured and theoretical peak-peak voltages can be found by assuming triangular waveforms and dividing the respective peak-peak voltages by $2\sqrt{3}$. They are found to be 31.1mV (measured) and 17mV (theoretical worst case).

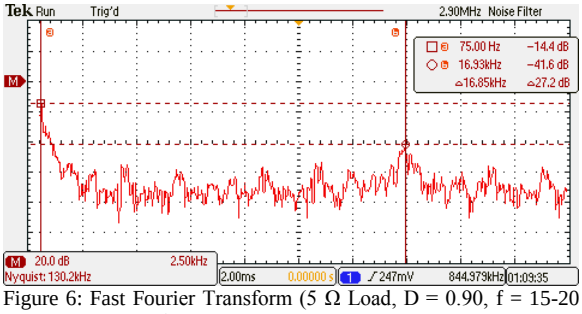


Figure 6: Fast Fourier Transform (5 Ω Load, D = 0.90, f = 15-20 kHz) (db Values of 120 Hz and 16.93 kHz Components Shown)

Fig. 6 shows a FFT of the output voltage Vout as determined by the measurement oscilloscope. There is a peak 75Hz which corresponds to the ripple in Vin (actually at 120 Hz) and a secondary peak at 16.93

kHz which is very close to the Buck converter switching frequency.

Comparing the ratio of the rms voltages is the same as comparing the ratio of their peak-peak voltages. For the 120Hz case that is 1.16 V as seen in Figure 4 and 0.108V from the cursor measurements in Figure 5. The ratio is 0.108/1.16 = 0.09 which can then be compared to the difference between the first and second peaks on the FFT, which equals -12.4dB – (-41.6dB) = -27.2dB = 0.043. This is not quite 0.09 however looking at Figure 6 we can see that there is a lot of noise making exact values hard to determine.

Next, the Vds transient in the Buck converter circuit is examined. Two cases are considered: one with the input ripple capacitor, and one without it. Fig. 7 shows the measured Vds waveform without the ripple capacitor. Fig. 8 shows the same voltage with the capacitor. It is seen that there is much less oscillation amplitude when the capacitor is present. Note that the vertical scale on the waveform shown in Fig. 8 is more magnified.

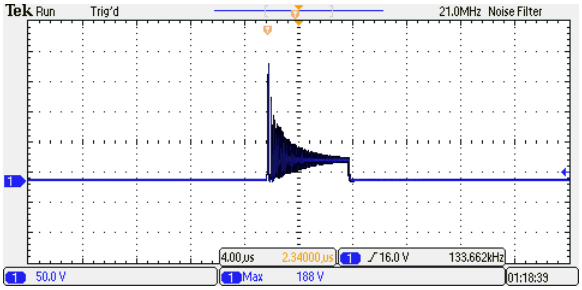


Figure 7: Case A - VDS without input ripple current capacitor

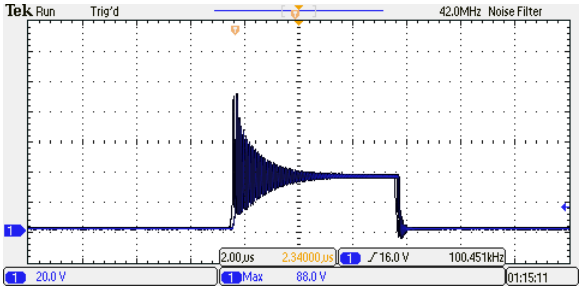


Figure 8: Case B - VDS with input ripple current capacitor

The Vds oscillation amplitudes with and without the capacitor are tabulated below.

	Without Cap	With Cap
Vds	181V	88V

Lastly, discontinuous current mode (DCM) operation of the Buck converter is examined. The duty cycle of the converter is reduced till the onset of DCM is evident from the appearance of low frequency oscillations in the voltage transient across the inductor. Figs. 9 and 10 show the inductor voltage transient in DCM operation. Figs. 11 and 12 show the same transient at the boundary between continuous and discontinuous operation.

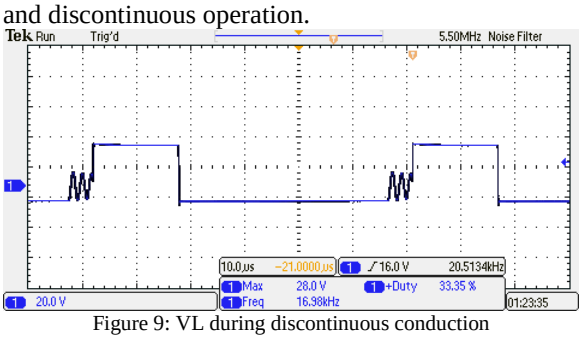


Figure 9: VL during discontinuous conduction

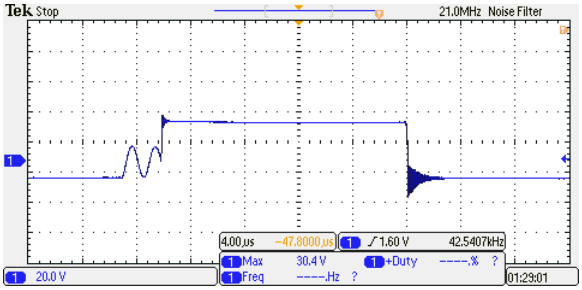


Figure 10: VL during discontinuous conduction, zoomed in view.

From the values of D, f, Vin, Iin, Vout, and Iout at the continuous / discontinuous boundary, the inductance L can be estimated. The values recorded are as follows.
D = 0.4
f = 16.9kHz
Vin = 36.5V
Iin = 1.42A
Vout = 13.92V
Iout = 2.86A

From these values L can be calculated using equation (6) [1].

$$L = \frac{V_{out}(1-D)}{2I_{out}} \qquad (6)$$

The resulting calculated value of L is 86.398uH. This compares favorably with the labeled value of 100uH.

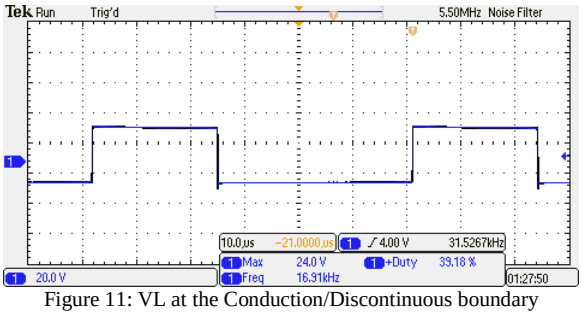


Figure 11: VL at the Conduction/Discontinuous boundary

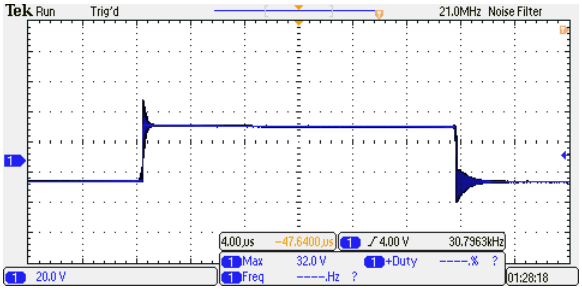


Figure 12: VL at the Conduction/Discontinuous boundary; zoomed in view.

Conclusion

The DC-DC Buck converter provides a simple way to convert a higher DC voltage to a lower DC voltage by utilizing a switch and voltage and current storage devices. One interesting property of this circuit is that it has two different modes, CCM and DCM. If designed properly (Inductor sized correctly), the Buck converter will always operate in CCM. The ability to change states, if desired, is an interesting concept but also dangerous if your load will not handle the DCM well. Lastly, we realize that the idealized assumptions we made about the Buck converter are just that, ideal assumptions. In practice, Vin could possess some ripple and unless the designer/manufacturer of the Buck converter is willing to pay for a very large capacitor, Vout and Iout will have some ripple. Also, we know that all components are not truly lossless, so there will be some power lost in the DC-DC conversion.

	Rounok	Jonathan
Circuit Build	50%	50%
Circuit Testing	50%	50%
Lab Report	60%	40%

References

[1] M. Flynn, "_Lab_Week_6_EE462L_DC_DC_Buck_2014_9_25.pdf", The University of Texas at Austin, Austin, TX, EE 462L: Power Electronics Laboratory course, Spring 2015. [Online]. Available: https://utexas.instructure.com/courses/1129504

EE462L – DC-DC Boost Converter

Team 255 – Rounok Joardar, Jonathan Lew

Spring, 2015

Circuit/Lab Overview

Very similar to the DC-DC Buck converter, the DC-DC Boost converter instead takes a DC input, and outputs a higher DC output voltage. Like the Boost converter, the Buck converter has two operation modes, continuous conduction mode (CCM), and discontinuous conduction mode (DCM). CCM is when the inductor current never dips below 0 A, it may momentarily reach 0 A, but never linger there. In DCM, the inductor current reaches and stays at 0 A, and the capacitor attempts to backfeed the inductor but is prevented by the freewheeling diode. In DCM, the power to the load is provided only by the capacitor. The Boost converter, because of its configuration, is also a much more sensitive circuit when compared to the Buck converter. If the duty cycle approaches one, the circuit will short Vin. Additionally, if there is no load connected to the Boost, then the capacitor voltage may exceed its rating.

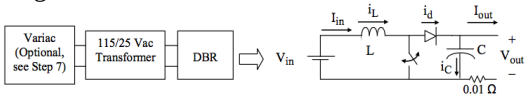


Figure 1: Boost Converter Schematic [1]

Circuit Testing

The boost converter shown in Fig. 1 is constructed and then tested in the manner described in this section. In all cases the output of the converter is connected to a 120V 150W light bulb. First, with the gate driver running at 90 kHZ the duty cycle D is increased to the point where the output dc voltage is about 120V. The values of D, Vin, Iin, Vout and Iout are as shown in Table 1.

Table 1. Summary data for boost converter switched at 90 kHz.

D	Vin (V)	Iin (A)	Vout (V)	Iout (A)
0.755	30.3	6.21	122.4	1.25

Theoretically, the relationship between Vout and Vin for a boost converter is given as [1]:

$$V_{out} = \frac{V_{in}}{1-D} \qquad (1)$$

From the data of Table 1, using Vin of 30.3 and D of 0.755 in equation (1) gives Vout = 123.7V. This compares very well with the measured dc output of 122.4V. Regarding power used and transferred by the converter, it is found that the total input power (Vin times Iin) is 188.163W. The output power (Vout time Iout) is 153W. The converter efficiency therefore is 153/188.163 = 81.3%. The converter loses efficiency due to I^2R losses and switching losses in the mosfet. As a result the mosfet heats up. The temperature of the mosfet after several minutes of operation was measured as 33.6°C.

Fig. 2 shows a screen shot of the voltage across the mosfet switch used in the boost converter.

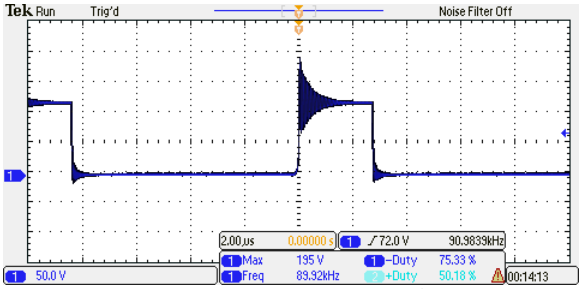


Figure. 2. Measured Vds at 90 kHz switching frequency. Vds is seen to be switching between about 120V and 0V. The peak voltage is 195V due to ringing when the mosfet turns off.

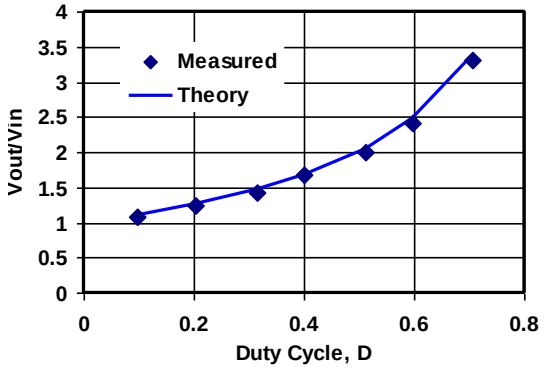


Figure. 3. Measured versus theoretical comparison of Vout/Vin ratio as a function of duty cycle D at a frequency of 90 kHz.

Fig. 3. shows the ratio Vout/Vin of the boost converter as a function of the duty cycle of the mosfet gate voltage at a 90 kHz switching frequency. Both measured and theoretically calculated values are shown. The measured Vout/Vin ratio overlaps with the theoretically expected result. In addition, it is noted that the converter circuit remains in continuous conduction mode (CCM) for the entire range of duty cycles measured above. The inductance required for the circuit to stay in CCM mode is given by [1]:

$$L_{boundary} = \frac{V_{in} D}{2 I_{in} f} \qquad (2)$$

For the range of D used, the maximum value of L from (2) was computed to be 45µH using the

recorded values of Vin and Iin. Since the inductor used in this circuit is larger, 100μH, it is normal that CCM operation was maintained throughout this experiment.

The above experiments were repeated at 30kHz switching frequency with a duty cycle around 75%. Table 2 shows the summary data for this case.

Table 2. Summary data for boost converter switched at 30 kHz.

D	Vin (V)	Iin (A)	Vout (V)	Iout (A)
0.756	30.18	6.45	120.7	1.25

Theoretically, using (1) and the data from Table 2, the expected output voltage is 123.7V. Once again it is found that the experimentally measured output voltage matches the theoretically calculated value very well. The measured efficiency in this case is 77.5%. This is slightly worse than the 90kHz case. As before, the efficiency loss is due to switching losses and heating losses. Because of increased I^2R losses in the mosfet, its temperature increased to 37.2°C.

The drop in efficiency and the higher temperature of the mosfet at 30kHz can be explained by considering the I^2R losses in the mosfet. The mosfet can be considered to have a constant on resistance. The rms current through the mosfet is given as [1]:

$$I_{rms,mosfet} = \sqrt{D\left(I_{in}^2 + \frac{\Delta I^2}{12}\right)} \qquad (3)$$

where ΔI is the ripple amplitude on the inductor current and is given as [1]:

$$\Delta I = \frac{DV_{in}}{Lf} \qquad (4)$$

where f is the switching frequency. Clearly, at lower frequencies the ripple amplitude of the inductor current will be higher. As a result, the rms current through the mosfet will be higher at lower frequencies (per eq. 3 and 4). Consequently, the I^2R losses in the mosfet will be higher leading to loss of converter efficiency and increase in mosfet temperature.

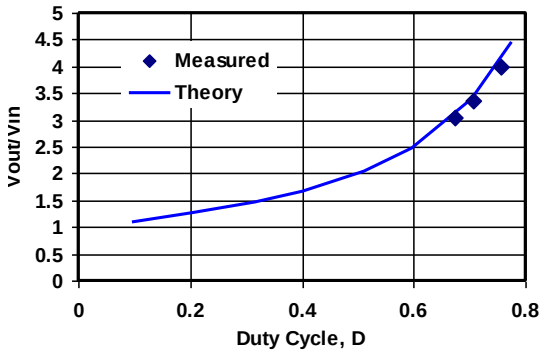


Figure. 4. Measured versus theoretical comparison of Vout/Vin ratio as a function of duty cycle D at a frequency of 30 kHz.

Fig. 4. shows the ratio Vout/Vin of the boost converter as a function of the duty cycle at a 30 kHz switching frequency. Both measured and theoretically calculated values are shown. The measured Vout/Vin ratio overlaps with the theoretically expected result. However, for 30kHz operation it was possible to measure Vout, Vin, etc. for only a few values of D because the converter went into discontinuous conduction mode (DCM) very quickly as D was reduced. This is not unexpected because the minimum L requirement, shown in eq. (2), goes inversely as frequency. At one-third the previous frequency the L would need to be three times higher. Otherwise, the inductor ripple current is three times larger, leading to earlier onset of DCM. Measurements showed that the onset of DCM happens approximately at D = 0.7. At this point, Vin = 31.54V and Iin = 4.36A. Using (2) gives a minimum L of 84.4μH which is reasonably close to the actual value of L used (100μH).

Using the above data from 30kHz operation, ΔI, rms inductor current, and rms capacitor current are computed. The values are as follows.

$$\Delta I = \frac{DV_{in}}{Lf} = 7.6A$$

$$I_{L,rms} = \sqrt{I_{in}^2 + \frac{\Delta I^2}{12}} = 6.81A$$

$$I_{C,rms} = \frac{\Delta I}{2\sqrt{3}} = 2.19A$$

Lastly, the boost converter is operated with solar cell input power. The load is still a 150W 120V light bulb. Fig.5 shows the measured and theoretical Vout/Vin versus D behavior. There is good agreement between measurement and theory.

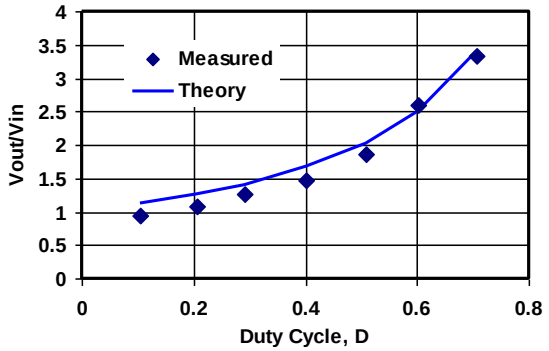


Figure. 5. Measured versus theoretical comparison of Vout/Vin ratio as a function of duty cycle D at a frequency of 90 kHz with solar cell input to boost converter.

Fig. 6 shows the output P-V behavior of the solar cell driven converter. The maximum power extracted is about 78W.

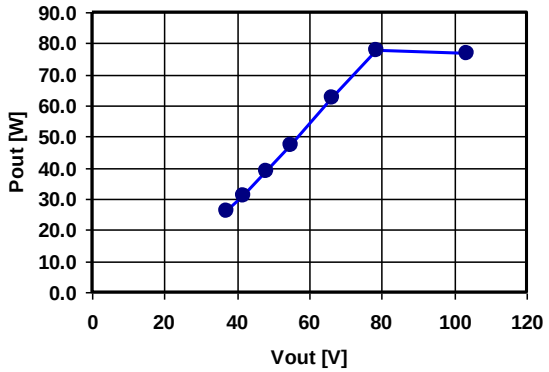


Figure. 6. Measured output P-V behavior with solar cell input power to boost converter.

Conclusion

While very similar to the Buck converter, the Boost converter even uses the same components as the Buck, the Boost is a very different circuit. Unlike the Buck, the Boost takes an input voltage and raises it while sacrificing current to the load. The Boost also makes it look like the load attached to it has a lower resistance to the source, while the Buck did the opposite. Lastly, the Boost converter is much less forgiving than the Buck converter, a no load condition or a high duty cycle puts the Boost converter at risk of harming itself by exceeding the ratings of its components.

	Rounok	Jonathan
Circuit Build	50%	50%
Circuit Testing	50%	50%
Lab Report	60%	40%

References

[1] M. Flynn, "_Lab_Week_7_EE462L_DC_DC_Boost_2014_9_25.pdf" , The University of Texas at Austin, Austin, TX, EE 462L: Power Electronics Laboratory course, Spring 2015. [Online]. Available: https://utexas.instructure.com/courses/1129504

EE462L – DC-DC SEPIC Converter

Team 255 – Rounok Joardar, Jonathan Lew

Spring, 2015

Circuit/Lab Overview

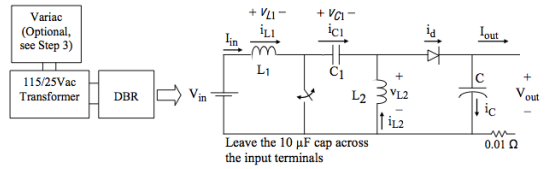


Figure 1: SEPIC Converter Schematic [1]

Circuit Testing

The SEPIC converter shown in Fig. 1 is constructed and then tested in the following manner. The converter input is attached to a DBR circuit generating about 35V DC. With the gate driver running at 90 kHZ the duty cycle D is gradually increased so that the output dc voltage is increases from 10V to about 90V. For output voltages between 10 and 20V a 5ohm resistive load is used. For 20V to 40V output a 10ohm resistive load is used. For outputs above 40V a 120V, 150W light bulb is used. The loads are changed in this manner to keep the power dissipation within the load's capability. The values of D, Vin, Iin, Vout and Iout are as shown in Table 1. Iin and Iout are obtained from the measured voltage drops across 0.01ohm shunt resistors connected to the input and output terminals.

Table 1. Summary data for SEPIC converter switched at 90 kHz.

D	Vin (V)	Iin (A)	Vout (V)	Iout (A)
0.35	35.42	0.8	10.0	2.05
0.44	33.36	3.16	19.67	4.0
0.47	33.25	3.53	29.92	3.01
0.55	31.29	6.65	39.69	3.9
0.5	34.58	1.52	50.0	0.77
0.55	34.1	2.05	60.3	0.9
0.67	33.66	2.66	70.2	1.12
0.7	33.13	3.37	81	1.22
0.74	32.24	4.17	91.5	1.33

Theoretically, the relationship between Vout and Vin for a boost converter is given as [1]:

$$V_{out} = \frac{D}{1-D} V_{in} \qquad (1)$$

From the data of Table 1, and using equation (1) the measured and theoretical performance of the SEPIC converter can be compared. Fig. 2. shows such a plot. There is good match between the measured and theoretical voltage ratio as D is varied.

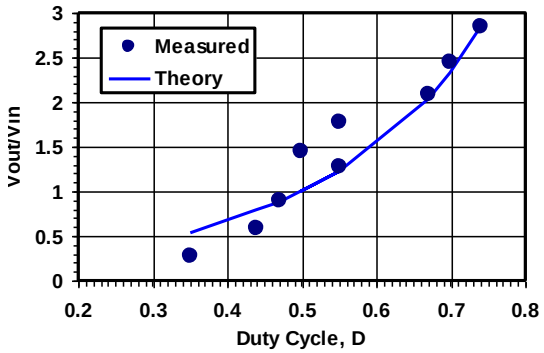
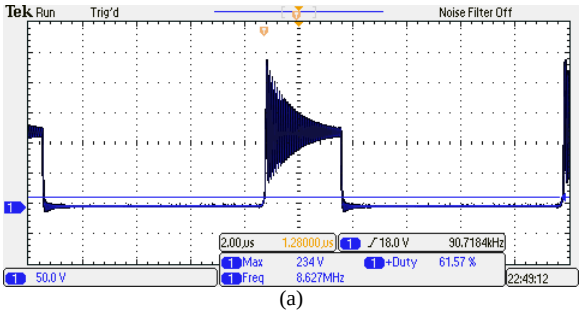
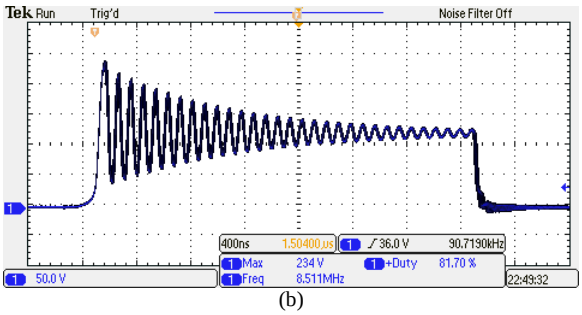


Figure. 2. Measured versus theoretical comparison of Vout/Vin ratio of the SEPIC converter as a function of duty cycle D at a frequency of 90 kHz.



(a)



(b)

Figure. 3. (a) Measured Vds at 90 kHz switching frequency. Vds is seen to be switching between about 120V and 0V. The peak voltage is 195V due to ringing when the mosfet turns off. (b) Close-up view of same waveform.

Fig. 3 (a) shows a screen shot of the voltage across the mosfet switch used in the SEPIC converter at 90V output. As expected, Vds switches between 0 and 130V (= Vin + Vout) ignoring the ringing. Fig. 3(b) is a close-up view of the Vds waveform.

Conclusion

References

[1] M. Flynn, "_Lab_Week_8_EE462L_DC_DC_SEPIC_2014_10_7.pdf", The University of Texas at Austin, Austin, TX, EE 462L: Power Electronics Laboratory course, Spring 2015, slide 15. [Online]. Available: https://utexas.instructure.com/courses/1129504