EE462L – H-Bridge Power Stage Lab

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Lab Overview

This lab is a continuation of the previous work on building and testing an H-Bridge power electronics circuit. Previously, we had only constructed the PWM control board for the H-Bridge circuit, but we now build the actual H-Bridge circuit itself. We attached the previously constructed PWM control board to the H-Bridge power circuit and use the two together to invert a 35-40VDC signal to a 60Hz AC waveform. A simplified figure of what the H-Bridge power circuit looks like can be seen in Fig. 1. The output from the H-Bridge is measured across a 5Ω load at different DC input voltages and using two separate triangle comparator frequencies.

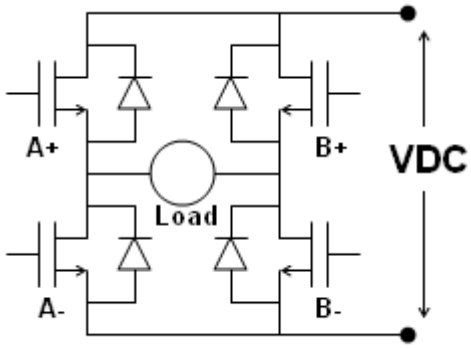

Fig. 1. H-Bridge inverter circuit made from four MOSFET switches. Freewheeling diodes are internal to the mosfets.

H-Bridge Gate Voltage Generation

The PWM output signals generated by the controller circuit constructed in the previous lab cannot be directly connected to the gates of the H-Bridge mosfets. The gate signals for the A+ and B+ mosfets (high side mosfets) need to be level shifted so that they are referenced to their source voltages. Also "dead time" needs to be added between the high side and low side gate signals to prevent the high side and low side mosfets from being on simultaneously (shoot through).

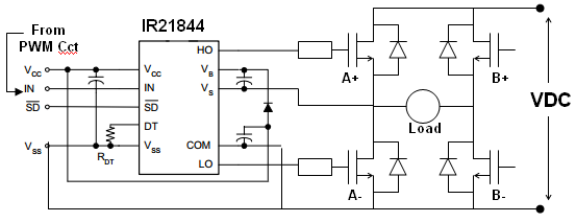

Fig. 2. Schematic showing gate drive signal generation for H-Bridge inverter circuit using IR21844 half bridge gate driver IC.

Connections to only the gates of left half of bridge are shown. Right half bridge is connected to an identical circuit.

Two half-bridge driver ICs (International Rectifier part 21844) are used to process the H-Bridge gate drive signals. A simplified schematic of how the PWM signal, gate driver circuit and H-Bridge are hooked up is shown in Fig. 2.

H-Bridge Measurements

This section describes the various measurements made after assembling the H-Bridge power stage PCB and connecting it to the controller PCB from the last lab.

Fig. 3 shows the measured signal at the gate of one of the mosfets with no load connected across the H-Bridge output. The control voltage on the PWM circuit is set to zero in this case. As expected, the waveform is a square wave (~ 50% duty cycle) because it is generated by comparing a symmetrical triangular wave with zero volts. The frequency of this signal is 139.4 kHz which is the frequency of Vtri in the PWM circuit. The height of the pulses is about 10V.

Fig. 4 shows the same gate signal with higher Vcont. Again, as expected, the pulse width narrows as Vcont increases because the triangular voltage Vtri is compared against a higher level. Unfortunately, there is a lot of jitter in the scope screen capture, possibly due to the effect of the lower frequency of Vcont.

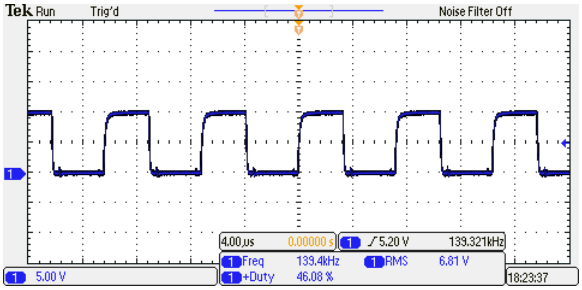

Figure. 3 Measured signal at mosfet gate with Vcont = 0 in the PWM controller circuit.

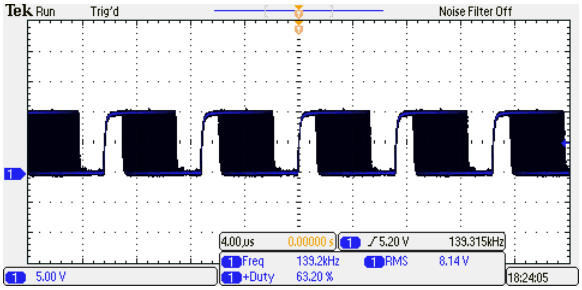

Figure. 4 Measured signal at mosfet gate with Vcont increased above in the PWM controller circuit. There is a lot of jitter in the waveform.

Next, a 5Ω load is attached across the H-Bridge output and its dc voltage is increased to 10V. The resulting voltage waveform at the inverter output is shown in Fig. 5. The frequency of the output signal is 60Hz, duty cycle is 49.42% (i.e. almost symmetric) and its peak to peak amplitude is about 15V. The RMS voltage as reported by the scope is 4.9V. A multimeter reading of the RMS output voltage was 4.85V which is very close to the scope estimate. The corresponding power dissipation is 4.8W.

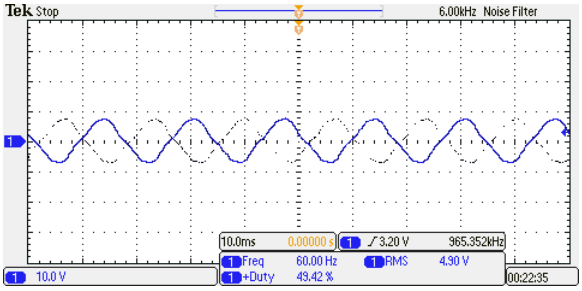

Figure 5. H-Bridge inverter output waveform with 5Ω load and 10V dc input. Frequency of inverter output is 60Hz and peak-peak amplitude is about 15V.

Fig. 6 shows the same H-Bridge inverter output waveform with but with the dc voltage increased to 35V. There is significant deterioration in the shape of the waveform possibly due to parasitic inductance in the wires and load resistor. The frequency of the output waveform is still 60Hz and the RMS voltage is 17.2V as reported by the scope. This corresponds to a power dissipation of 59.2W. On a multimeter the RMS reading is 19.73V which corresponds to a somewhat larger power dissipation of 77.9W. The mosfet heat sinks felt slightly warm to touch.

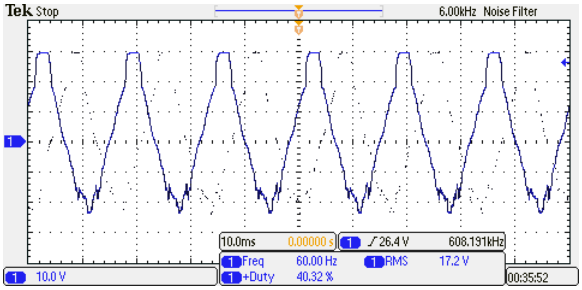

Figure 6. H-Bridge inverter output waveform with 5Ω load and 35V dc input. Frequency of inverter output is 60Hz and peak-peak amplitude is about 54V.

Next, in order to improve the shape of the output voltage waveform at high dc input, the carrier frequency in the PWM controller was reduced by increasing the CF capacitor in the controller circuit to 4.7nF. This reduces the frequency of Vtri to 44 khZ. It is expected that at lower frequency some of the parasitic effects would be less leading to a cleaner waveform. Results are as shown in Fig. 7. The waveform is definitely cleaner compared to Fig. 6. The frequency is 60Hz, peak to peak amplitude is about 52V, and RMS voltage reported by the scope is 16.8V which is a bit lower than in the previous case. This RMS voltage corresponds to a power dissipation of 56.4W in the 5Ω resistor. Interestingly, the RMS reading on a multimeter increased to 22.3V in this case which implies a power dissipation of 99.5W in the 5Ω load resistor.

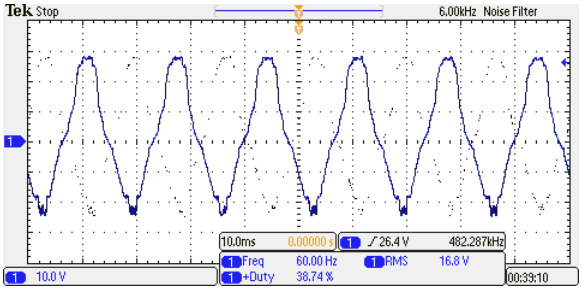

Figure 7. H-Bridge inverter output waveform with 5Ω load and 35V dc input. Frequency of inverter output is 60Hz and peak-peak amplitude is about 52V.

Conclusions

This is the first time we see the full H-bridge circuit in action. Previously, we had only seen the control circuit, which takes care of the pulse width modulation and creates an inverse control signal to control both legs of the H-bridge. We see that at a low input voltage the output of the H-bridge is very sinusoidal, but when raising the DC input voltage,

inductance in the 5Ω power resistor seriously distorts the output signal. One way to remedy this is to reduce the switching events by lowering the frequency of Vtri. A slight improvement in the output waveform can be seen by lowering the frequency of Vtri via the 4.7nF CF capacitor, but not enough to offset the inductance of the load.

	Rounok	Jonathan
Circuit Build	65%	35%
Circuit Testing	50%	50%
Lab Report	50%	50%

References

[1] M. Flynn, "_Lab_Week_11_EE462L_H_Bridge_Inverter_Power_Stage.pdf", The University of Texas at Austin, Austin, TX, EE 462L: Power Electronics Laboratory course, Spring 2015, slide 15. [Online]. Available: https://utexas.instructure.com/courses/1129504