EE462L – DC-DC SEPIC Converter

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Circuit/Lab Overview

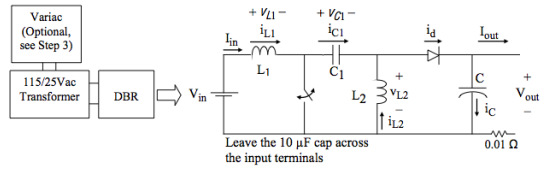


Figure 1: SEPIC Converter Schematic [1]

Circuit Testing

The SEPIC converter shown in Fig. 1 is constructed and then tested in the following manner. The converter input is attached to a DBR circuit generating about 35V DC. With the gate driver running at 90 kHZ the duty cycle D is gradually increased so that the output dc voltage is increases from 10V to about 90V. For output voltages between 10 and 20V a 5ohm resistive load is used. For 20V to 40V output a 10ohm resistive load is used. For outputs above 40V a 120V, 150W light bulb is used. The loads are changed in this manner to keep the power dissipation within the load's capability. The values of D, Vin, Iin, Vout and Iout are as shown in Table 1. Iin and Iout are obtained from the measured voltage drops across 0.01ohm shunt resistors connected to the input and output terminals.

Table 1. Summary data for SEPIC converter switched at 90 kHz.

D	Vin (V)	Iin (A)	Vout (V)	Iout (A)
0.35	35.42	0.8	10.0	2.05
0.44	33.36	3.16	19.67	4.0
0.47	33.25	3.53	29.92	3.01
0.55	31.29	6.65	39.69	3.9
0.5	34.58	1.52	50.0	0.77
0.55	34.1	2.05	60.3	0.9
0.67	33.66	2.66	70.2	1.12
0.7	33.13	3.37	81	1.22
0.74	32.24	4.17	91.5	1.33

Theoretically, the relationship between Vout and Vin for a boost converter is given as [1]:

$$V_{out} = \frac{D}{1-D} V_{in} \qquad (1)$$

From the data of Table 1, and using equation (1) the measured and theoretical performance of the SEPIC converter can be compared. Fig. 2. shows such a plot. There is good match between the measured and theoretical voltage ratio as D is varied.

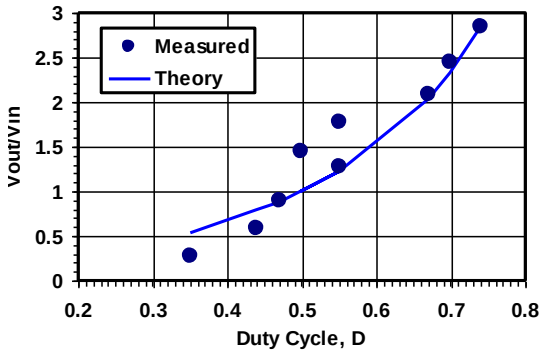
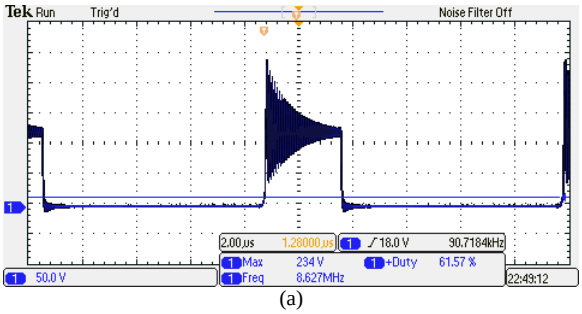
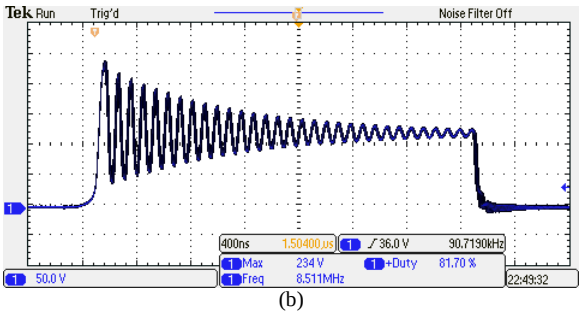


Figure. 2. Measured versus theoretical comparison of Vout/Vin ratio of the SEPIC converter as a function of duty cycle D at a frequency of 90 kHz.



(a)



(b)

Figure. 3. (a) Measured Vds at 90 kHz switching frequency. Vds is seen to be switching between about 120V and 0V. The peak voltage is 195V due to ringing when the mosfet turns off. (b) Close-up view of same waveform.

Fig. 3 (a) shows a screen shot of the voltage across the mosfet switch used in the SEPIC converter at 90V output. As expected, Vds switches between 0 and 130V (= Vin + Vout) ignoring the ringing. Fig. 3(b) is a close-up view of the Vds waveform.

Conclusion

References

[1] M. Flynn, "_Lab_Week_8_EE462L_DC_DC_SEPIC_2014_10_7.pdf", The University of Texas at Austin, Austin, TX, EE 462L: Power Electronics Laboratory course, Spring 2015, slide 15. [Online]. Available: https://utexas.instructure.com/courses/1129504